

Hazeltine 1500 SERIES

VIDEO DISPLAY TERMINALS
MAINTENANCE MANUAL

Part Numbers 4DTD155207
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4DTD155255-1
4DTD155260
4DTD155260-1

HI-1053A
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Hazeltine Corporation
COMPUTER TERMINAL EQUIPMENT
GREENLAWN, N.Y. 11740 (516)549-8800
TELEX 96-1435

SAFETY SUMMARY

WARNING

Dangerous voltages (15 K vdc and 115 vac) are present in the Video Display Terminal and may remain present in the monitor circuits after power is removed. Use caution when working on internal circuits. Do not work alone.

Use caution when handling the cathode-ray tube (eg, wear safety goggles to avoid risk of implosion. The internal phosphor coating is toxic; if the tube breaks and skin or eyes are exposed to phosphor, rinse with cold water and consult a physician.

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SECTION 1

INTRODUCTION AND DESCRIPTION

1.1 INTRODUCTION

1.1.1 This manual provides maintenance instructions for the Hazeltine 1500, 1510 and 1520 terminals. Only the domestic models are covered in the body of the manual. Difference data for export units is provided in Appendix C. The symbol # in the body of the manual indicates an item which is different in the export units.

1.1.2 The 1500 model may have one of two logic/keyboard assemblies. Part number 4DTD155202 is unique to the 1500. Part number 4DTD155246-() is a common board shared by the 1500, 1510 and 1520 (unused parts are not installed) with different dash numbers employed for the different models. Differences between the '202 board and the common board (mostly reference designations) are noted on the diagrams and a separate schematic is provided in Appendix B.

1.1.3 The contents of this manual are subject to change without prior notice and may not reflect latest changes in the product. Confirmation and any required clarification of this information can be obtained from your Hazeltine sales representative. Additional information is provided in the Reference Manuals.

1.2 GENERAL DESCRIPTION

1.2.1 Model 1500

The terminal is a self-contained unit with keyboard, logic, monitor, and power supplies in a single chassis. It is compatible with a variety of interface requirements and permits extensive remote control of display functions. Technical characteristics are summarized in table 1-1.

1.2.2 Remote commands to the terminal must be preceded by a ~ (tilde) to identify what follows as a remote command. Exceptions are cursor right, backspace, and tab; these do not require a lead-in character. Terminal controls and indicators are listed in table 1-2 and illustrated in figure 1-1.

Table 1-1. Technical Characteristics

<p>DISPLAY FORMAT</p> <p>Screen:</p> <p>Capacity:</p> <p>Character Format:</p> <p>Cursor:</p> <p>Character Set:</p> <p>#Refresh Rate:</p> <p>Display:</p> <p>TV Line Standard:</p>	<p>12 inch (30.5 cm) diagonal, P4 phosphor</p> <p>80 characters/line x 24 lines (1920 characters)</p> <p>7 x 10 dot matrix in 9 x 11 dot window</p> <p>Triangle on base (▲), cursor and character blink alternately when superimposed. (1500 units with '202 logic board have block cursor)</p> <p>94 displayable ASCII. All 128 ASCII codes can be keyed</p> <p>60 Hz, non interlace</p> <p>White on black or black on white (switch selected) two display intensity levels</p> <p>308 lines/frame, 264 lines displayed</p>
<p>INTERFACE</p> <p>Input/Output:</p> <p>Transmission Rates:</p> <p>Parity:</p> <p>Character:</p> <p>Modes</p> <p>1500:</p> <p>#1510/1520:</p> <p>Printer Buffer (1520):</p>	<p>EIA RS-232C compatible with Western Electric type 103A modem, or 20 to 40 mA current loop (switch selected)</p> <p>110, 300, 1200, 1800, 2400, 4800, 9600, or 19,200 baud (switch selected)</p> <p>Odd, even, 1 or 0 (switch selected)</p> <p>10 or 11 bits (start, seven bit ASCII, parity, one or two stop bits), number of stop bits = two for 110 baud, = one for all others</p> <p>Full duplex or half duplex</p> <p>Full duplex, half duplex, format or format/local</p> <p>Parallel TTL level with strobe, or serial EIA with strobe (switch selected), at 110, 300 or 1200 Baud (switch selected)</p>
<p>PHYSICAL/ENVIRONMENTAL DATA</p> <p>Size:</p> <p>Weight:</p> <p>Power Required:</p> <p>Temperature Range:</p> <p>Humidity Range:</p>	<p>15-1/2 inches (39.4 cm) wide, 13-1/2 inches (34.3 cm) high, 20-1/2 inches (52.2 cm) deep</p> <p>35 pounds (16 kg)</p> <p>104 to 126 v, 60 Hz ±1%, 120 watts</p> <p>10° to 40°C (50° to 104°F) operating, -20° to 65°C (4° to 150°F) storage</p> <p>5% to 90%, non-condensing</p>
<p>KEYBOARD FEATURES</p> <p>Typamatic Operation:</p>	<p>All alphanumeric, symbol, space and cursor control keys repeat at 15 char/second rate when depressed longer than 0.8 second</p>
<p>REMOTE COMMANDS</p> <p>1500/1510/1520:</p>	<p>Cursor up, down, right, left, home</p> <p>Insert line, delete line</p> <p>Clear screen, clear to end of screen, clear to end of line, clear foreground, clear to end of screen (background)</p> <p>Intensity control (set foreground, set background)</p> <p>Keyboard lock, keyboard unlock</p> <p>Alarm</p>

Table 1-1. Technical Characteristics (cont)

1510/1520:	<p>Tab (Cursor tabs over background data to next foreground field)</p> <p>Direct cursor address, send cursor address</p> <p>Set format, return to switches</p> <p>Set transmit mode (protected, or protected and unprotected; and batch, page or line)</p> <p>Remote transmit</p> <p>Back tab</p> <p>Send status (terminal sends to bit status word defined below)</p>																				
1520:	<p>Set print mode: (1) Remote print (causes all data to be sent to printer starting from last print position, or top of screen if no previous print, and ending at cursor position when command received). (2) On line print with display (all transmitted and received data printed except commands with ~ lead in). (3) On line print without display (Same as (2) except received data is not displayed, and received commands are not executed (except terminate on line print and send status). Keyboard remains active and keyboard entries are displayed)</p> <p>Terminate on line print</p>																				
Terminal Status Word:																					
Bit	Status																				
0*	1 = Buffer empty																				
1*	1 = Printer on line																				
2 3	<table border="1"> <thead> <tr> <th colspan="4">Format Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Half or</td> <td>0</td> <td>Batch</td> <td>1</td> <td>Page</td> <td>1</td> <td>Line</td> </tr> <tr> <td>0</td> <td>full duplex</td> <td>1</td> <td></td> <td>0</td> <td></td> <td>1</td> <td></td> </tr> </tbody> </table>	Format Mode				0	Half or	0	Batch	1	Page	1	Line	0	full duplex	1		0		1	
Format Mode																					
0	Half or	0	Batch	1	Page	1	Line														
0	full duplex	1		0		1															
4	1 = Parity error in previous transmission received																				
5 6	<table border="1"> <thead> <tr> <th colspan="4">Termination Character</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>CR</td> <td>0</td> <td>ETX</td> <td>1</td> <td>EOT</td> <td>1</td> <td>None</td> </tr> <tr> <td>0</td> <td></td> <td>1</td> <td></td> <td>0</td> <td></td> <td>1</td> <td></td> </tr> </tbody> </table>	Termination Character				0	CR	0	ETX	1	EOT	1	None	0		1		0		1	
Termination Character																					
0	CR	0	ETX	1	EOT	1	None														
0		1		0		1															

* Always 0 for 1510

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NOTE: For Model 1500 units with the 202 Logic Board, the EIA/CUR LOOP positions are the reverse of those shown.

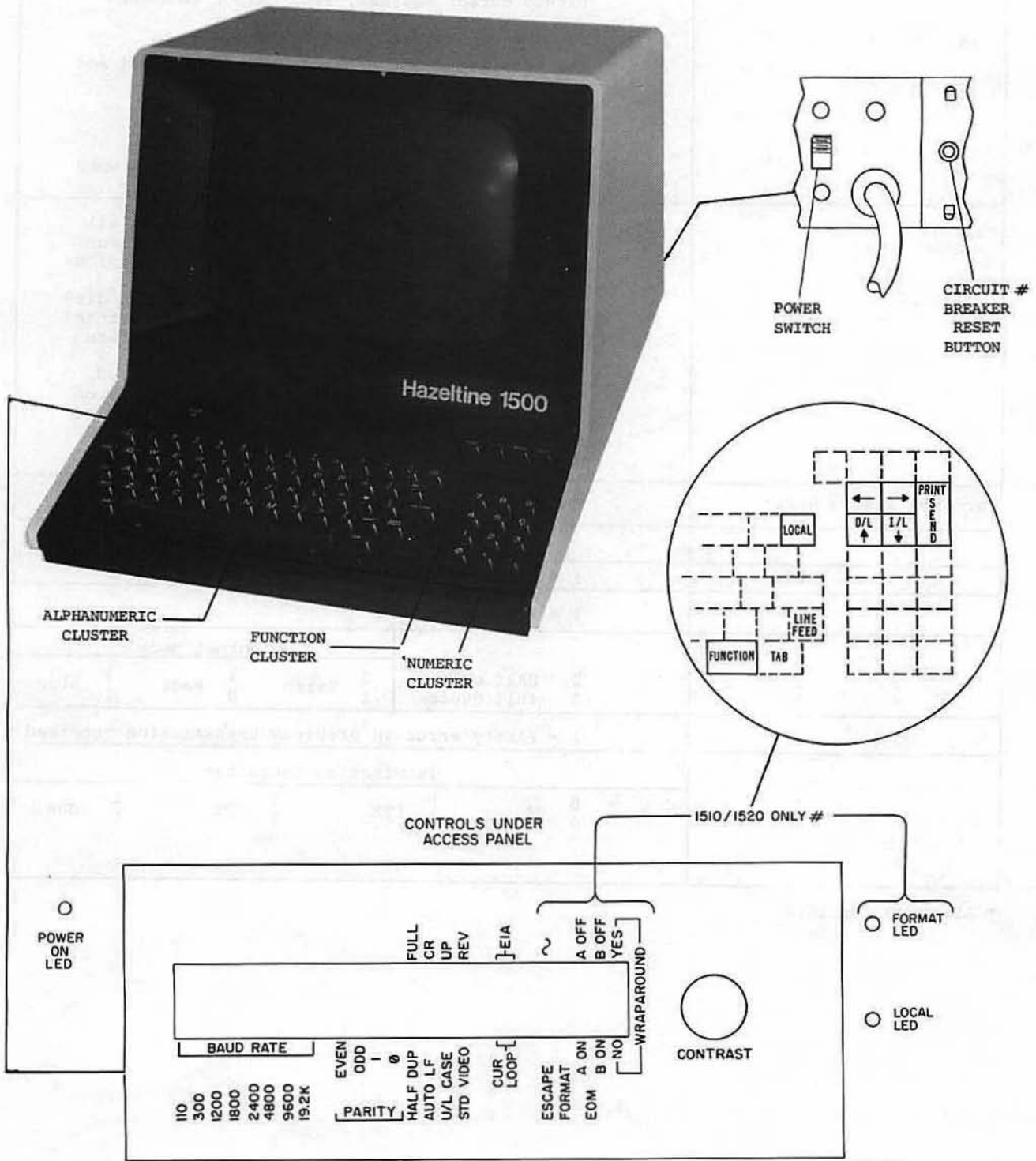


Figure 1-1. Controls and Indicators

Table 1-2. Controls and Indicators

Controls and Indicators Under Access Panel (figure 1-1)																
#BAUD RATE	One of eight switches set to on (forward) to select desired rate.															
PARITY	One of four switches set to on (forward) to select parity mode. ODD or EVEN selection causes odd or even parity bit to be generated for each character transmitted and the same parity is checked for each character received. A parity error is indicated by an audible alarm and P _E is displayed. 1 or 0 selection causes a 1 or 0 in the parity bit position of each character transmitted. No parity check is performed on received data.															
HALF DUP/FULL	Select full or half duplex operation.															
AUTO LF/CR	When AUTO LF is selected, a carriage return causes the cursor to advance to the beginning of the next line. A line feed causes no change in cursor position. When CR is selected, a carriage return causes the cursor to move to the beginning of the present line. A line feed causes the cursor to move down one line. (Overridden in FORMAT mode - AUTO LF operation is automatic).															
U/L CASE/UP	When UP case is selected, all alphabetical characters are transmitted and stored as upper case regardless of the SHIFT key position. Keyboard ALL CAPS switch is overridden. When U/L CASE is selected, characters are controlled by the keyboard SHIFT or ALL CAPS keys.															
STD VIDEO/REV	Selects standard display (white characters on black screen) or reverse video (black characters on white screen).															
EIA/CUR LOOP (2 switches)	Enables the EIA or current loop interface. Both switches must be set to same position.															
CONTRAST	Adjusts contrast to operator preference.															
POWER ON	Light-emitting diode (red). Indicates when power is on.															
1510/1520 ONLY																
ESCAPE/~	Selects either the ASCII ESC code or ~ character as the lead in for remote commands.															
FORMAT	Selects format mode (if set, terminal will go to format mode at turn on, after reset, or after return-to-switches command). In this mode, keyboard data is stored and displayed, but not transmitted, when entered. Transmission is controlled by send command (keyboard or remote).															
EOM switches (2)	Select character to be inserted as end-of-message character at the end of a transmission: <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;"><u>EOM A</u></th> <th style="text-align: left;"><u>EOM B</u></th> <th style="text-align: left;"><u>EOM Character</u></th> </tr> </thead> <tbody> <tr> <td>ON</td> <td>ON</td> <td>CR</td> </tr> <tr> <td>OFF</td> <td>ON</td> <td>EOT</td> </tr> <tr> <td>ON</td> <td>OFF</td> <td>ETX</td> </tr> <tr> <td>OFF</td> <td>OFF</td> <td>None</td> </tr> </tbody> </table>	<u>EOM A</u>	<u>EOM B</u>	<u>EOM Character</u>	ON	ON	CR	OFF	ON	EOT	ON	OFF	ETX	OFF	OFF	None
<u>EOM A</u>	<u>EOM B</u>	<u>EOM Character</u>														
ON	ON	CR														
OFF	ON	EOT														
ON	OFF	ETX														
OFF	OFF	None														

Table 1-2. Controls and Indicators (cont)

1510/1520 ONLY (cont)	
WRAPAROUND	YES: Cursor will automatically wrap around from the last column of one row to the first column of the next row when data is entered (except on bottom row in format mode). NO: Cursor will not wrap around and alarm will sound. A carriage return must be entered to move the cursor to the next line (or other cursor control).
FORMAT light	Lighted whenever terminal is in format mode. Blinks during batch transmissions and during "FUNCTION" operation.
#LOCAL light	Lighted while terminal is in local mode.
Keyboard Controls	
BREAK	Causes a 200 to 250 ms interruption on transmit data line.
RESET	Resets the keyboard lock and set foreground flags. Display of data is inhibited while key is depressed.
CLEAR	CLEAR : clears entire display to foreground spaces (In FORMAT mode, functions only when cursor is in home position) ^S CLEAR : clears all foreground data to foreground spaces ^C CLEAR : clears all data from, and including, cursor position to end of line to foreground spaces ^{CS} CLEAR: clears all data from, and including, cursor position to end of screen to foreground spaces
HOME	Homes cursor to row 0 column 0
ALL CAPS	Alternate action switch. When depressed, causes all alphabetic characters to be upper case regardless of SHIFT key position. When released (UP), permits upper or lower case as controlled by SHIFT key unless internal UP CASE/U/L switch is set for UP CASE. Data received as lower case is displayed as lower case.
Alphanumeric Cluster	Generates codes for characters and functions as marked.
Numeric Cluster	Duplicates same functions as corresponding keys in alphanumeric cluster but in adding machine arrangement. Key functions are not modified by control or shift keys.
Keyboard Controls (1510/1520 Only)	
FUNCTION	Special purpose key to allow communication without affecting display. After FUNCTION key is pressed the next character entered will be transmitted in a two or three character sequence: ESC, character keyed, EOM character (if selected). Nothing will be stored or displayed. The FORMAT light will blink until the transmission is completed. An erroneous entry may be cancelled by depressing the FUNCTION key a second time.

Table 1-2. Controls and Indicators (cont)

Keyboard Controls (1510/1520 Only) (cont)																					
<p>SEND (Format Mode Only)</p> <p>PRINT (1520 only) (^SSEND) (Format or half duplex modes)</p> <p>LOCAL (Functions only in format mode)</p> <p>+ + + +</p> <p>I/L D/L</p>	<p>Initiates transmission in mode for which terminal has been conditioned (paragraph 1.2.5)</p> <p>^CSEND initiates line transmission regardless of preconditions.</p> <p>^{CS}SEND initiates page transmission regardless of preconditions.</p> <p>Initiates transmission to printer when not in printer on line mode. A print symbol (■) is displayed at present cursor position. All data from last print symbol (or top of screen if no previous print) to present cursor position, except data to right of CR or ■, is sent to printer. Cursor is advanced to start of next line (unless on bottom line).</p> <p>Puts terminal in local mode. Input data and commands will be ignored by terminal (but will be sent to printer if on line). Terminated by a SEND or by a second depression of LOCAL key. Used to permit formatting data without interference from received data.</p> <p>Move cursor up, down, right or left without affecting data stored in memory.</p> <p>Insert line/delete line. Same functions on 1500 require keying ^Cz and ^Cs respectively.</p>																				
Controls and Indicator at Rear of Chassis (figure 1-1)																					
<p>Power Switch and #Circuit Breaker</p>	<p>Switches AC power (down for on). Circuit breaker button pops out when actuated (1.75 amps). Push in to reset.</p>																				
Switches on Printer Buffer (1520 only) (figure 1-2)																					
<p>S1</p>	<p>Selects parallel or serial output and baud rate (S1-4 not used)</p> <table border="1"> <thead> <tr> <th></th> <th>S1-1</th> <th>S1-2</th> <th>S1-3</th> </tr> </thead> <tbody> <tr> <td>Parallel</td> <td>Up</td> <td>Up</td> <td>Up</td> </tr> <tr> <td>Serial-110 baud</td> <td>Up</td> <td>Up</td> <td>Down</td> </tr> <tr> <td>Serial-300 baud</td> <td>Up</td> <td>Down</td> <td>Down</td> </tr> <tr> <td>Serial-1200 baud</td> <td>Down</td> <td>Down</td> <td>Down</td> </tr> </tbody> </table>		S1-1	S1-2	S1-3	Parallel	Up	Up	Up	Serial-110 baud	Up	Up	Down	Serial-300 baud	Up	Down	Down	Serial-1200 baud	Down	Down	Down
	S1-1	S1-2	S1-3																		
Parallel	Up	Up	Up																		
Serial-110 baud	Up	Up	Down																		
Serial-300 baud	Up	Down	Down																		
Serial-1200 baud	Down	Down	Down																		

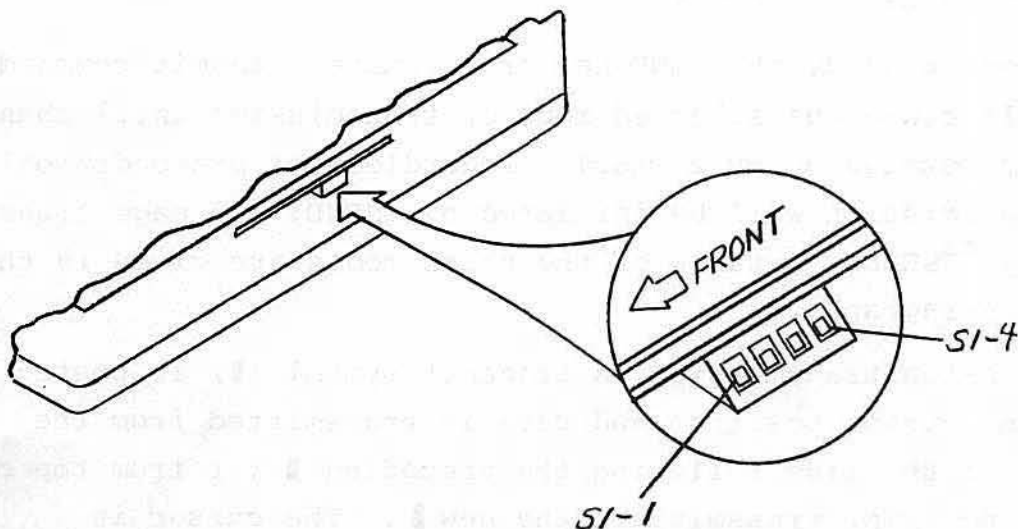


Figure 1-2. Switch S1 on Printer Buffer

1.2.3 Model 1510

The model 1510 contains all the features of the 1500, plus format and format/local mode capability. Additional remote commands are shown in table 1-1. Additional controls are listed in table 1-2.

1.2.4 Remote commands to the 1510 may use either a \sim or ASCII ESC (escape) character as a lead in. The \sim notation is used in this manual to designate the lead in character but it is to be understood the ESC must be substituted if that character is selected.

1.2.5 In the format mode, data is stored and displayed as entered, but not transmitted. Transmission is initiated by the SEND key or by remote command (there is a 10 ms delay after remote command). Only unprotected (foreground) data is transmitted unless the terminal has been preconditioned to send both protected and unprotected data, either locally or remotely ($\sim +$). The terminal will return to the send-unprotected-only mode after RESET, or after a remote command to do so (\sim comma). Data to the right of a CR or transmit symbol (■) is not sent. The FORMAT light blinks for the duration of the transmission, which may be by batch, page or line. The batch mode is automatically selected at turn-on and after a RESET. Other modes may be selected locally or by remote commands:

```
Set line transmit =  $\sim$  period
Set page transmit =  $\sim$  (
Return to batch   =  $\sim$  %
```

Once preconditioned, the SEND key or a remote transmit command (\sim SO) will cause the selected mode of transmission until changed by another command or by a RESET. Regardless of preconditioning, a line transmission will be initiated by c SEND, and page transmission by cs SEND. Details of the three modes are given in the following paragraphs.

1.2.6 In batch transmission, a transmit symbol (■) is posted at the present cursor position and data is transmitted from the beginning of the line following the preceding ■ (or from top of screen if no prior transmit) to the new ■. The cursor is

advanced to the start of the next line unless it is already on the bottom line, in which case it is placed at the beginning of the bottom line. New data may be entered immediately but the following commands cannot be entered until transmission is completed (FORMAT light stops blinking): TAB, ^STAB, all CLEARs, FUNCTION, all SEND key functions, I/L, D/L, LOCAL. The alarm will sound if any of these keys are depressed.

1.2.7 In line transmission, data on the cursor position line is transmitted from the beginning of the line and ends at a carriage return or the last none-space character on the line. The cursor is advanced to the start of the next line, with rollup if already on the bottom line, except no rollup will occur if the bottom line contains a protected character (cursor will be placed at start of line). Data entry following send command is the same as batch transmission.

1.2.8 In page transmission, all 24 lines are transmitted and the cursor is placed at the start of the bottom line. No rollup will occur. Data cannot be entered until the transmission is completed.

1.2.9 The format/local mode may be selected by depressing the LOCAL key when in format mode. Operation is the same format mode except no input data or commands will be accepted by the terminal. However, if a printer is on-line (1520 only) incoming data will be transferred to the printer. The LOCAL light will be on whenever the terminal is in that mode. Local mode is terminated by any SEND or by a second depression of the LOCAL key.

1.2.10 The 1510 model has cursor control keys (↑→←) primarily for use in format mode, although they function in full or half duplex as well. In format mode, the BACK SPACE and ^SBACK SPACE (DLE) will store the corresponding character at the cursor position and move the cursor right one position.

1.2.11 Model 1520

The model 1520 contains all the features of the 1510, plus a printer buffer with storage capacity for a full screen of data.

The printer buffer has full synchronizing capability for controlling a printer with either parallel or serial data transmission.

1.2.12 Three modes of operation are available: printer on line with display, printer on line without display, and printer off line. Printer on line may be initiated from a switch on the printer (or any means of grounding the printer on line switch input pin at the terminal), or by remote command. Either is sufficient to keep the printer on line. Both must be reset for off line operation. A remote on line print command is cancelled by a remote terminate on line print command ($\sim?$), or by a RESET (but the printer will remain on line (with display) if the printer on line switch input is true (low)).

1.2.13 In both on line modes, all data transmitted and received on the I/O channel is also sent to the printer via the printer buffer, except commands preceded by a \sim . Commands preceded by an ESC character are sent to the printer. If the terminal is in format mode, a line feed is inserted after each carriage return transmitted.

1.2.14 The printer on line with display mode may be initiated by the remote command $\sim/$, and on line without display by $\sim*$. In the latter case, received data is not displayed and the only inputs the terminal will respond to are send status ($\sim-$) and terminate on line print ($\sim?$). The keyboard remains active and data entered by keyboard will be stored and displayed.

1.2.15 In the off line mode, printing is controlled by the PRINT key ($\overset{S}{\text{SEND}}$) or by remote command ($\sim\text{RS}$). Transfer of data to the printer is similar to batch transmission except both protected and unprotected data is printed.

1. The print symbol (■) is posted at the initial cursor position and at the next adjacent character position. It is possible for the print symbol to wraparound (i.e., occupy the last character position on a line and the first character position of the following line).

2. The cursor moves to the first character position of the line following the previous print symbol, or the beginning of the screen if there is no intervening print symbol.

3. From the starting point data is transferred to the printer buffer at a very rapid rate independent of the printer rate. Transfer of data to the printer at the print rate is under control of the printer buffer.

4. At the end of each character line a CR code followed by a line feed code is generated before reading the first character of the following line. If the cursor encounters a CR code in the print field, it transfers the CR and line feed codes before the first character of the following line is read. Single transmit symbols are handled in the same manner as carriage returns. Data to the right of a CR or **█** is not sent.

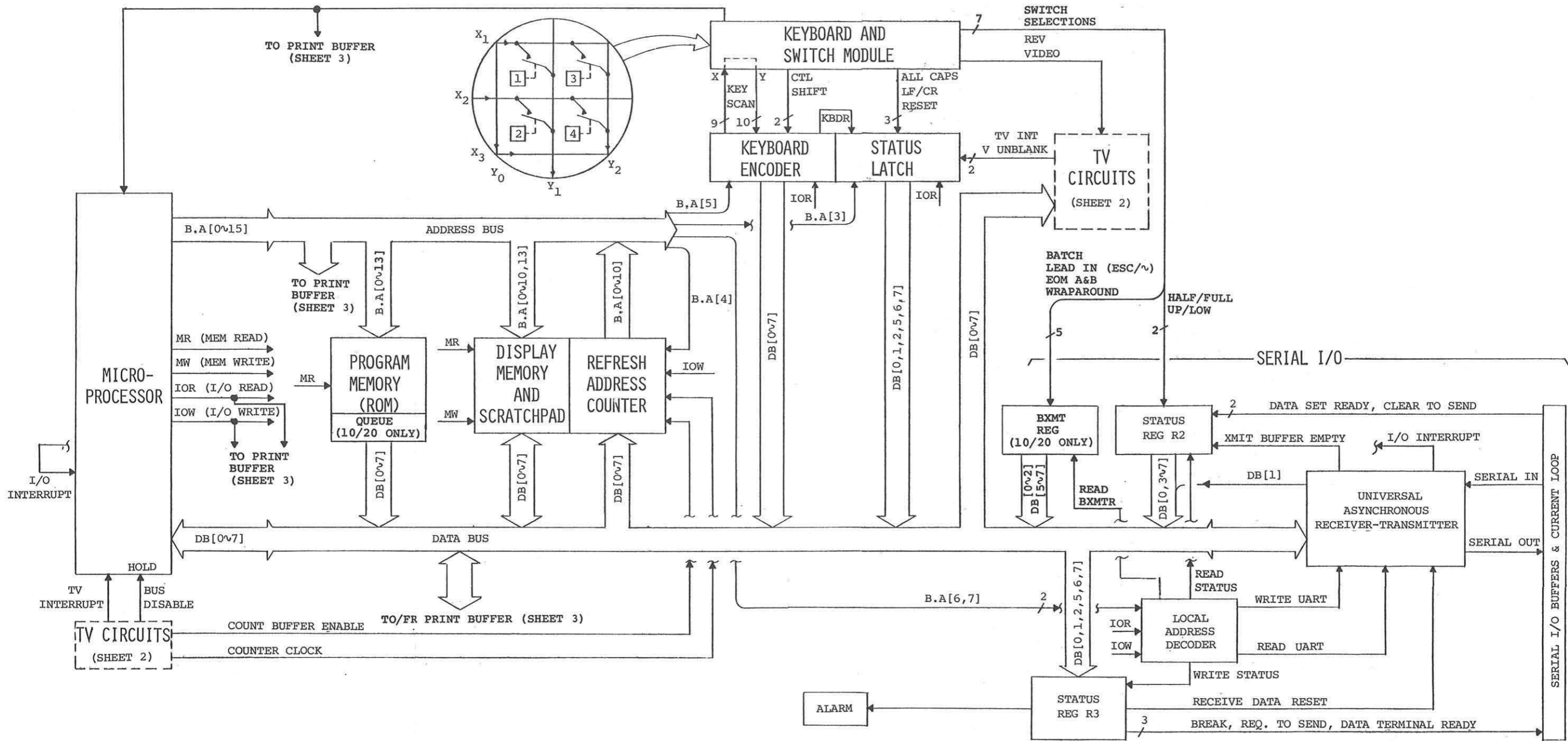
5. Readout ends at the print symbol posted at the beginning of the cycle. A CR/line feed is transmitted and the cursor moves to the first character position on the following line.

1.3 THEORY OF OPERATION

1.3.1 Introduction

Figure 1-3 is a functional block diagram showing the relationship of the major functional subdivisions of the terminal. The central element of the terminal is the microprocessor, which is connected to the other functional circuits by a 16-bit address bus, an 8-bit data bus, and four read/write control lines. The bits on the address bus are designated B.A[0] through B.A[15]. Bit 15 is not used. The data bus bits are designated DB[0] through DB[7].

1.3.1.1 The program for the microprocessor is stored in a read-only memory. Additional temporary memory for the microprocessor is available in a scratchpad, which is part of the same memory used to store the display characters. The microprocessor uses the scratchpad to stack data for a partially completed routine when it jumps to a subroutine and for storing input characters (input queue). The memory address structure is shown in figure 1-4.



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Figure 1-3. Terminal, Block Diagram (Sheet 1 of 3)

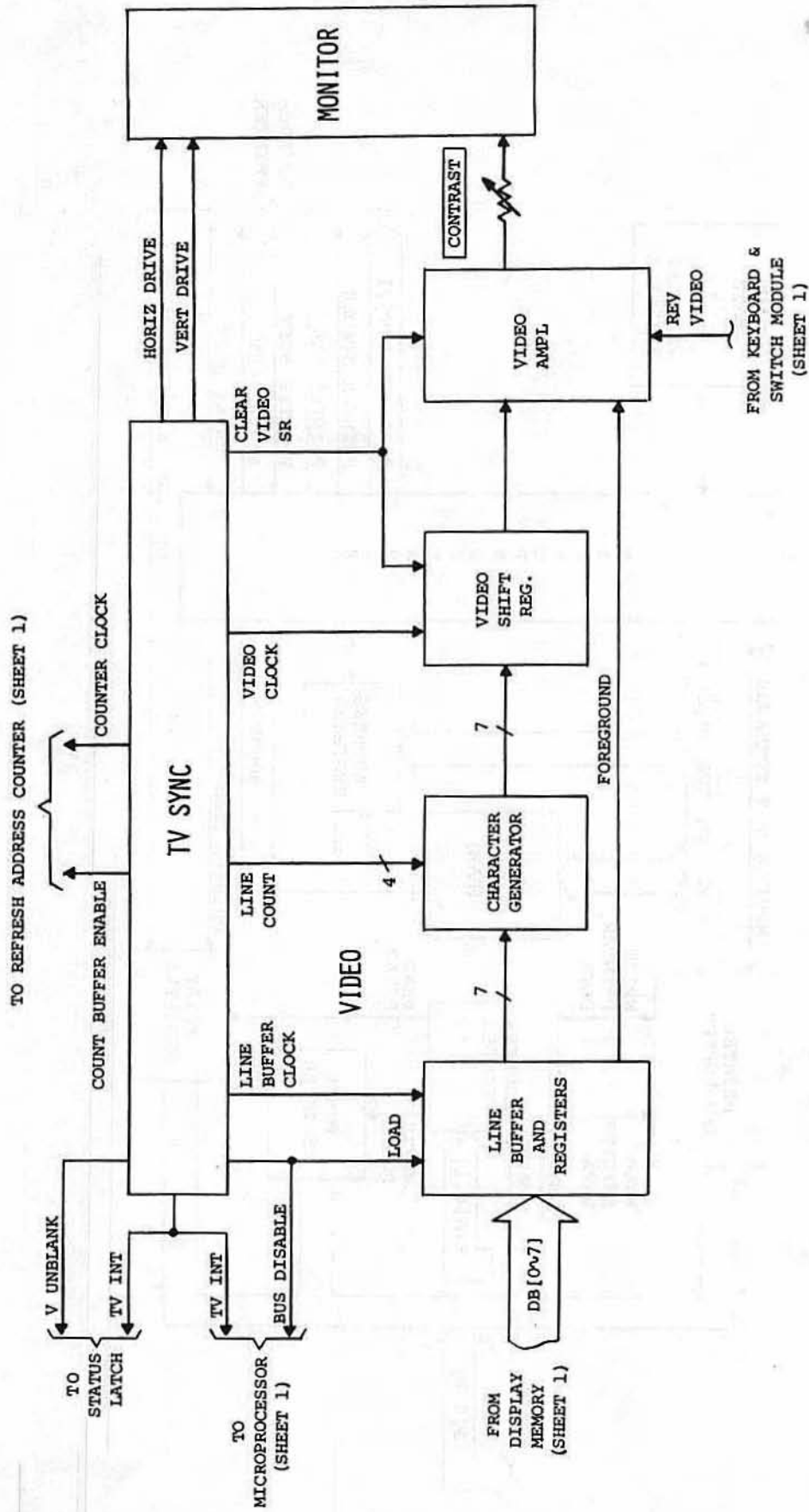


Figure 1-3. Terminal, Block Diagram (Sheet 2 of 3)

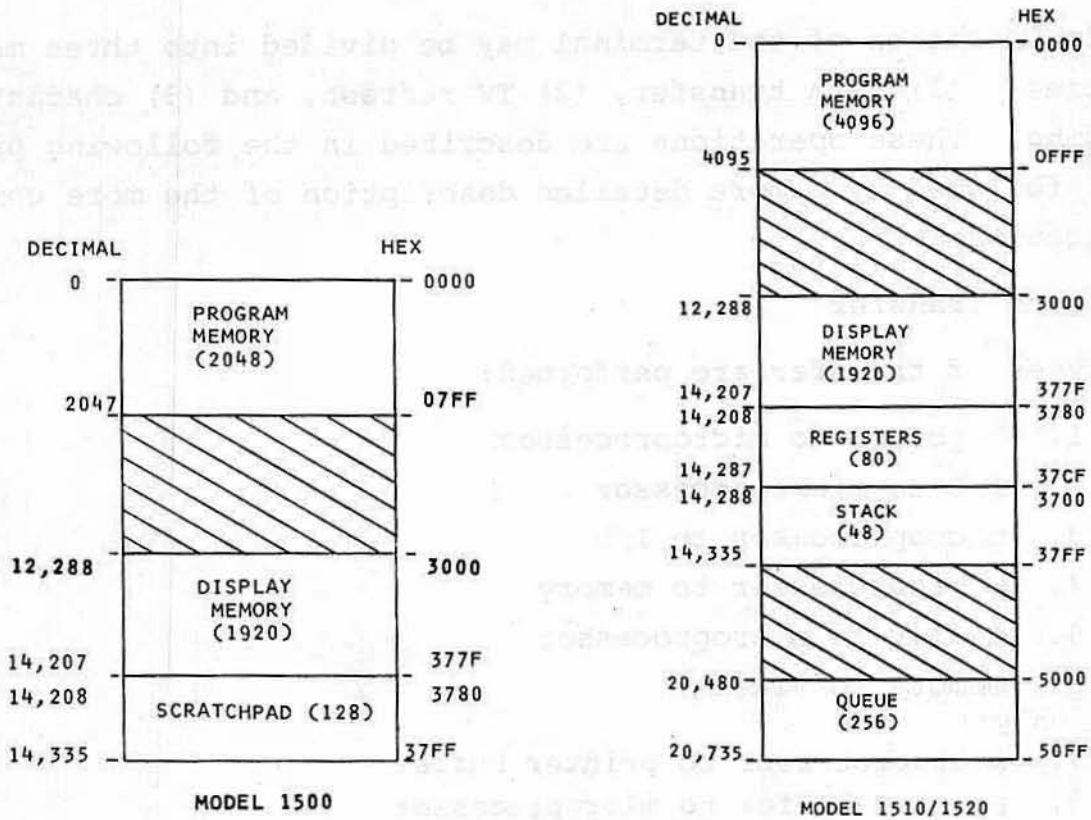


Figure 1-4. Memory Address Structure

The 1510 and 1520 models have an additional 256 x 8 queue, used for storage of all input characters, and for output characters in batch transmission mode. The address structure for input/output (I/O) is simpler since there are only five addresses. Address bits are used to address I/O, with one or two bits low (logic 0) designating a particular unit as follows:

<u>I/O Unit</u>	<u>Bit(s) Low</u>
Keyboard Status Latch (Read only)	B.A[3]
Refresh Address Counter (Write only)	B.A[4]
Keyboard Encoder (Read only)	B.A[5]
UART	B.A[6]
I/O Status (R2 if read, R3 if write)	B.A[7]
Batch Transmit Status Register (Read only)	B.A[6&7] (1510/1520)
Print Buffer	B.A[0] (1520)
Printer Control/Status (PCNTL if write, PSTAT if read)	B.A[1] (1520)

1.3.1.2 Operation of the terminal may be divided into three major categories: (1) data transfer, (2) TV refresh, and (3) character processing. These operations are described in the following paragraphs, followed by a more detailed description of the more complex circuits.

1.3.2 Data Transfer

Eight types of transfer are performed:

1. keyboard to microprocessor
2. I/O to microprocessor
3. microprocessor to I/O
4. microprocessor to memory
5. memory to microprocessor
6. memory to video
- (1520 only:)
7. microprocessor to printer buffer
8. printer buffer to microprocessor

All but one are controlled by the microprocessor. Control of transfer from display memory to the video circuits is shared by the tv sync circuits and the microprocessor.

1.3.2.1 Keyboard to Microprocessor. Each character key is located at a unique junction of 9 scan lines (designated X) and 10 output lines (designated Y). The keyboard encoder continuously excites the 9 scan lines, one at a time, and looks for a signal at the output lines. When a key is depressed a unique XY combination is recognized, which, in combination with the control and/or shift keys, addresses a memory location in the keyboard encoder in which the appropriate 8-bit character code is stored. When any character is detected, a keyboard data ready (KBDR) signal is applied to the status latch. The microprocessor periodically reads the status latch condition (IOR and B.A[3] low) and, when the KBDR condition is read, enters the keyboard service routine. The microprocessor then reads the keyboard data (IOR and B.A[5] low) transferring the character code to the microprocessor. If the same character is input two successive times with less than a 6 milli-second interval, it will be rejected. This prevents accidental

double entries due to switch bounce. Otherwise the character will be processed as appropriate for the modes and switch options in effect.

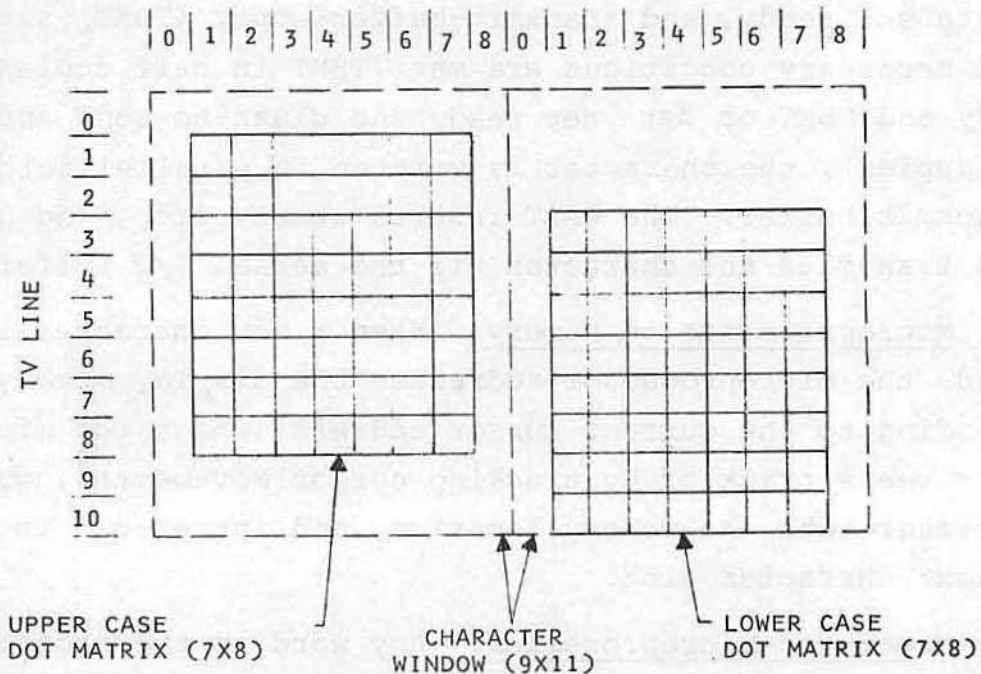
1.3.2.2 I/O to Microprocessor. The universal asynchronous receiver-transmitter (UART) is continuously ready to accept serial inputs. When a serial input is received, the UART stores it in an input buffer and generates an I/O interrupt signal. This causes the microprocessor to interrupt whatever it is processing and do a data I/O service routine. The UART is addressed and the character transferred to the microprocessor in parallel on the data bus (7 bit ASCII plus a 1 for DB[7] if a parity error is detected by the UART). The microprocessor then updates status register R3 with a receive data reset bit, which, in turn, resets the UART I/O interrupt signal.

1.3.2.3 Microprocessor to I/O. When a character is ready to be transmitted, the microprocessor enters a send character subroutine. Status register R3 is updated with a request-to-send bit which is transmitted via the serial I/O buffer. The microprocessor then reads status register R2 to determine the status of the clear-to-send, data set ready, and transmit-buffer-empty (TBMT) signals. When the necessary conditions are met (TBMT in half duplex; data set ready and TBMT or data set ready and clear-to-send and TBMT in half duplex), the character is written in parallel into the UART transmit buffer. The UART inserts start, stop, and parity bits and transmits the character via the serial I/O buffers.

1.3.2.4 Microprocessor to Memory. When a new character is to be displayed, the microprocessor addresses the display memory location corresponding to the current cursor address (which the microprocessor keeps track of by tracking cursor movements), writes the character into the memory location, and increments the cursor to the next character slot.

1.3.2.5 Memory to Microprocessor. Any word in the program memory or the display memory can be transferred to the microprocessor by a memory read command along with the appropriate address as indicated in figure 1-4.

1.3.2.6 Memory to Video. Transfer of display data to the video circuits, which store one row of characters at a time, is synchronized under control of the tv sync circuits. Each character occupies an 11 tv line window as shown in figure 1-5. At the beginning of line 10 of each 11 line character row, the tv sync circuits generate a bus disable signal. This signal causes the microprocessor to go to a hold status. The bus drivers are set to the high impedance state, reserving the address and data buses for transfer of the display data. The same signal enables the line buffer to load the data. A count buffer enable (CTBEN) signal enables the refresh address counter, which then controls the address bus. Eighty counter clock (CNTCLK) inputs to the counter cause 80 consecutive characters to be transferred to the line buffers. At this time, the bus disable signal is discontinued and control of the buses is returned to the microprocessor. Since 11 tv lines are required to display a complete character row, no display data transfer is required until line 10 of the next row. At the beginning of line 2 of each row, a tv interrupt signal is generated. This signal causes the microprocessor to



7704039

Figure 1-5. Character Format

interrupt whatever it is doing and enter a tv service routine. The microprocessor then calculates the address, in display memory, of the start of the next row to be refreshed (the microprocessor counts tv interrupts to keep track of where the tv refresh is). This address is written into the refresh address counter in preparation for the transfer of the next row. The address is transferred on the data bus DB [0 ~ 7], but into counter locations corresponding to address bits B.A[3 ~ 10]. The least significant four bits in the counter [0 ~ 3] are set to 0. The resolution of the address load is 16, which is adequate because all starting addresses are multiples of 16 ($80 = 16 \times 5$).

1.3.3 TV Refresh

1.3.3.1 The tv circuits block diagram is shown in sheet 2 of figure 1-3. Transfer of a row of characters to the line buffers was described above. The tv sync circuits divide and decode from an internal 33.264 MHz oscillator to produce the various timing signals needed to synchronize the display. The line buffer clock causes a new character code to be transferred from the buffers to the character generator every 9 tv dot intervals. The character generator is programmed with the dot pattern for each displayable character. The character code, plus the decoded line count, addresses the dot pattern for a particular line of the character. The dot pattern is then transferred in parallel to the video shift register. The video shift register clocks the video serially through the video amplifier to the monitor. The video amplifier output is at medium intensity for background characters, and high intensity for foreground characters, determined by the most significant bit of the character code in the line buffer.

1.3.3.2 At the end of each line and during vertical retrace, a clear video shift register (CLR VID SR) signal clears the shift register and disables the video amplifier input. This signal is a composite of either horizontal or vertical blanking. The character codes stored in the line buffers are recirculated eleven times (line number 0 through 10) and a new row is loaded at line ten.

1.3.4 Data Processing

1.3.4.1 All data processing is performed by the microprocessor by performing the program stored in program memory. The program consists of four primary modules (Executive, Keyboard Service, Filter, and Initialize), an interrupt subroutine, and several detail subroutines. Flow Charts for the model 1500 program are shown in figure 1-6. Table 1-3 explains abbreviations used in the flow charts.

1.3.4.2 The overall program flow is shown on sheet 1 of figure 1-6. At power turn-on, or when the RESET button is pressed, the initialize routine is performed. This clears old data from storage and sets up the microprocessor initial conditions. The screen is cleared for a power up reset, but not for a pushbutton reset. The executive routine is then entered. This program causes the processor to look for work, and is repeated continuously until interrupted by an "interrupt" input. An interrupt causes the INTRP subroutine to be performed. If the interrupt is a tv interrupt, it services the tv refresh function described in paragraph 1.3.3; if it is an I/O interrupt, it transfers an I/O character to the input queue. Data in the processor registers is pushed into the scratchpad while the interrupt is serviced. After the interrupt, the data from the scratchpad is popped back into the registers and the interrupted routine is resumed. An I/O service may be interrupted by a tv interrupt. In this case, the I/O data is pushed down, the tv refresh is serviced, and the I/O servicing is resumed. When the EXEC routine is performed, the queue is checked for a character to be processed. If a character is available, the filter module is entered. This module performs the actions appropriate for the particular character, calling subroutines as necessary. When the filter routine is concluded, the executive routine restarts. If no character is in the queue, the keyboard is checked (unless in keyboard lock condition). If a keyboard character is available, the KBSVC (keyboard service) routine is performed. This routine includes double-entry prevention. If a key is held down, only one entry will be made until

Table 1-3. Terms and Abbreviations Used in Program Flowcharts

Abbreviation/Name	Description or Usage
ALCNT Alarm Count	Used to time audible alarm. Set to 20 when BEL character is decoded or a parity error is detected. Decremented by each vertical unblank.
BKCNT Break Counter	Used to time break. Set to 14 when BREAK key is decoded. Decremented by vertical unblanking.
CA	Flag raised when request-to-send is output (EIA CA signal).
CADDR Cursor Address	Refresh memory location corresponding to present cursor position.
CI Cursor Interchange Flag	Set when cursor is over a character other than space. Used to control interchange of cursor and character.
CICNT Cursor Interchange Counter	Used to time interchange of cursor and character. Set to 20 when cursor is moved to character position and to 10 each time an interchange is implemented. Decremented by each vertical unblank.
CURSX, CURSY Cursor X and Cursor Y address	Character number (X) and row number (Y) of present cursor position as measured from left or top of display.
CX Flag	Set when X part of direct cursor address command has been implemented. Used to indicate that next address will be Y.
EOC End of character	Signal from UART when last bit of a character has been transmitted from serial output buffer. Used to determine start of delay at end of half duplex transmission.
FLAG 1, FLAG 2 (1500) Flag Registers No. 1 and No. 2	Number 1 stores Lead In, RA, CX, CI, Pass 1, Pass 2, Foreground, and KBLOK flags. Number 2 stores CA, Alarm, Break, and data ready reset flags.
FLAGS 1 through 7 (1510/1520)	Status flags.
KBCNT Keyboard Count	Used to track time a key is held down. Set to 48 on 1st pass (delay) and to 4 on 2nd pass (repeat rate). Decremented by each vertical unblank. Reset when key released.
KBLOK F Keyboard Lock Flag	Set by keyboard lock character ($\sim^C U$). Reset by keyboard unlock command or initialize module. Keyboard will not be read when set.
KCHAR Keyboard Character	Last keyboard character. Used for comparison with present keyboard character to determine if same or new character.
LEADP Queue leading pointer	Address in buffer at which next I/O character is to be stored. Incremented as each character is stored. Reset when end of buffer is reached. See TRALP.
LOP Line zero pointer	Number of rows, from start of refresh memory to memory location of top line of display. Used with RLP to calculate starting memory address for next line to be refreshed. Incremented with each rollup.
PASS 1, 2 Keyboard pass flags	Indicates number of consecutive times the same character is read from keyboard. Used to prevent double entries and control typamatic operation.
RA Read cursor address flag	Set when a command to send cursor address is received.
RLP Refresh Line Pointer	Number of the next row to be refreshed. Incremented at each tv interrupt. Reset to 0 each vertical retrace. Used to control the starting point of the refresh memory address counter at the start of each row.

Table 1-3. Terms and Abbreviations Used
in Program Flowcharts (cont)

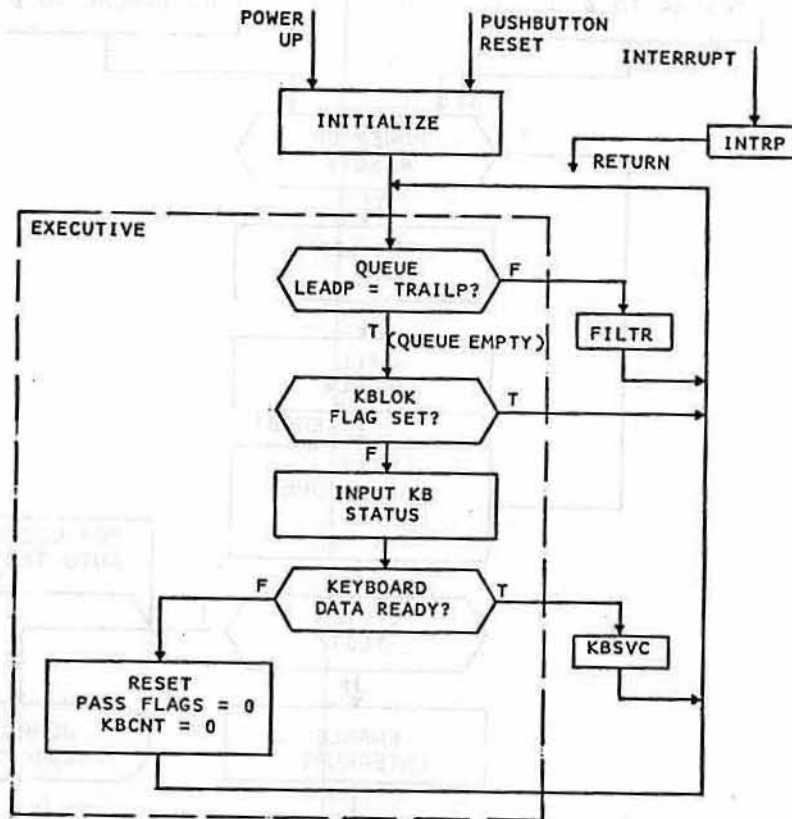
Abbreviation/Name	Description or Usage
TAB PASS 1	Set during tab. Used to limit search for background foreground (unprotected) field.
TBMT Transmit buffer empty	Signal from UART indicating that serial output buffer is empty.
TMPST Temporary storage register	Register (located in scratchpad) used for temporary storage during a particular routine.
TRALP Queue trailing pointer	Address in buffer of oldest I/O character not processed. Incremented as character is stored.
XCNT	Count used to control blinking of FORMAT lamp during transmit.

approximately 0.8 second (48 vertical unblankings) and typamatic operation will then be performed. The routine is shown on sheet 4 of figure 1-6. The tables noted in the flow chart are conversion charts for lower case to upper case and keyboard encoder to ASCII. On completion of the keyboard service, the executive routine is restarted. The subroutines used to implement the various terminal functions are shown in the flow charts. In reading the flow charts, the following terms and conventions should be understood.

- o A (D) or (H) following a number indicates decimal or hexi-decimal notation.
- o A module (sheets 1 through 4) ends with an exit which specifies the routine to start next. A subroutine ends with a "return" which exits to the point from which the subroutine was called.
- o A "call" inserts the subroutine called into the flow of the calling routine. The calling routine is resumed when the subroutine is completed. A "jump" terminates the routine. If the jump is to a subroutine, the exit from the subroutine resumes the routine from which the calling routine was called.

Executive and Index

MNEMONIC	FUNCTION	SHT	MNEMONIC	FUNCTION	SHT
ADJCP	Adjust cursor position	8	FILTER	Filter	3
CBEOS	Clear to end-of-screen (background)	6	FTAB	Foreground Tab	15
CHOME	Home cursor	7	ILINE	Insert line	9
CISAV	Save character in cursor interchange register	8	INITIALIZE	Initialize	2
CLEFT	Cursor left	7	IN QU	Transfer character to input queue	13
CLEOL	Clear to end-of-line	6	INTRP	Interrupt	5
CLEOS	Clear to end-of-screen	6	KBSVC	Keyboard service	4
CLFG	Clear foreground	15	LF	Line feed	10
CLSCR	Clear screen	6	PTR	Pointer	6
CR	Carriage return	10	RADDR	Direct cursor address	11
CURDN	Cursor down	7	ROLUP	Rollup	9
CURMA	Cursor memory adjust	8	SADDR	Send cursor address	13
CURUP	Cursor up	7	SEND CHAR	Send character to UART	12
DLINE	Delete line	9	YMA	Calculate Y memory address	14
EXEC	Executive	1			



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Figure 1-6. Flowcharts (Sheet 1 of 16)

Initialize

RST0:

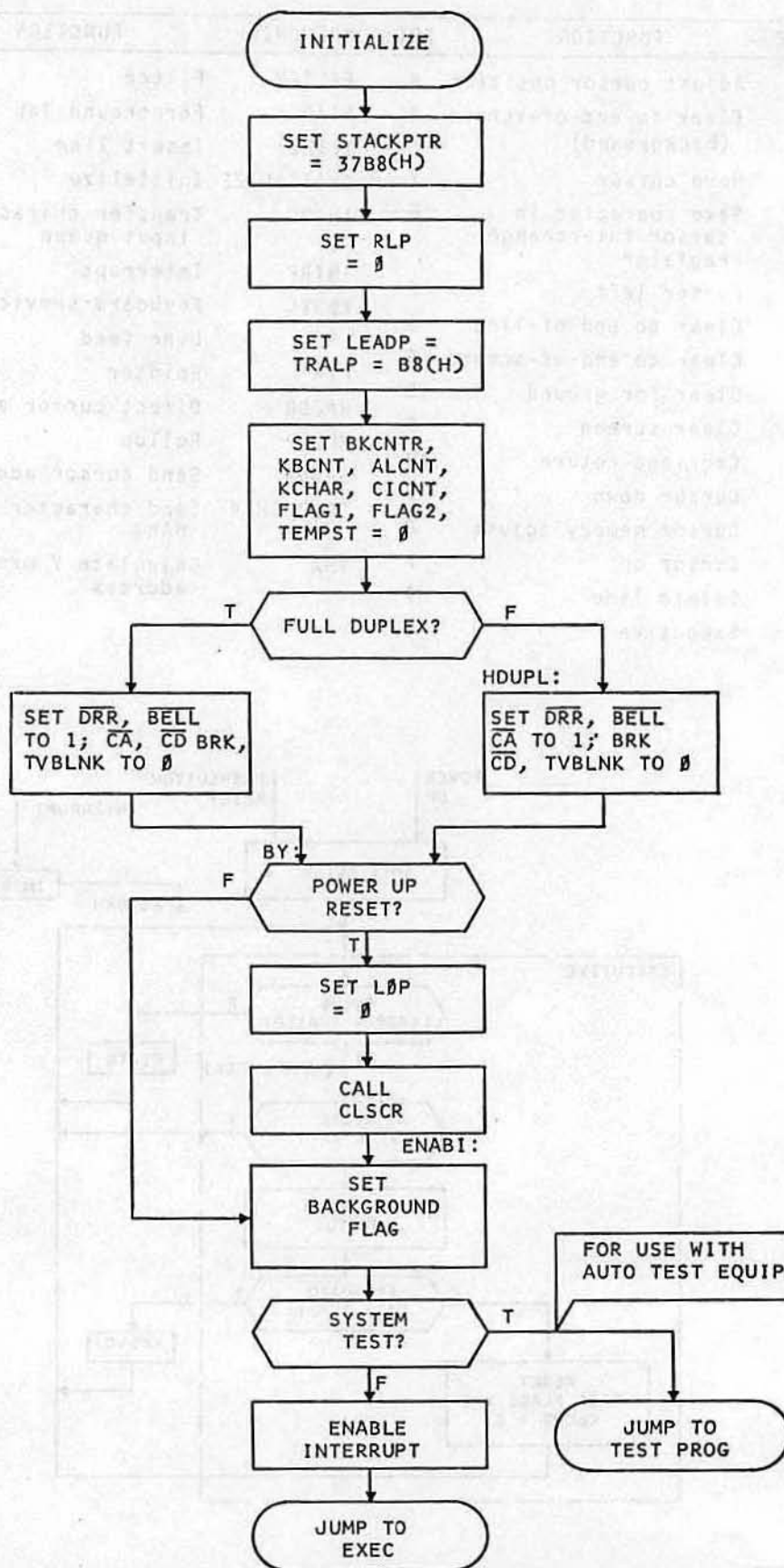
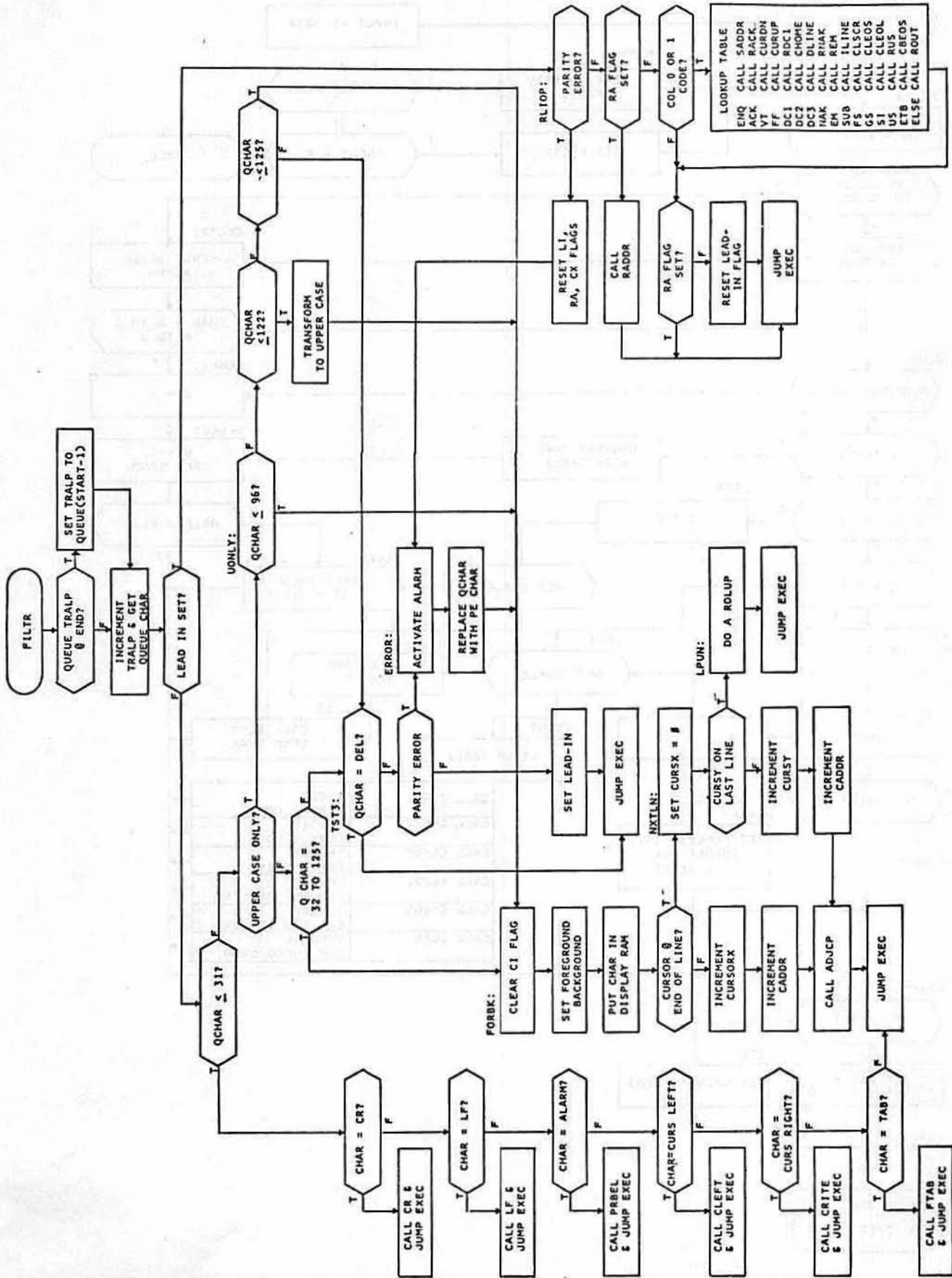


Figure 1-6. Flowcharts (Sheet 2 of 16)

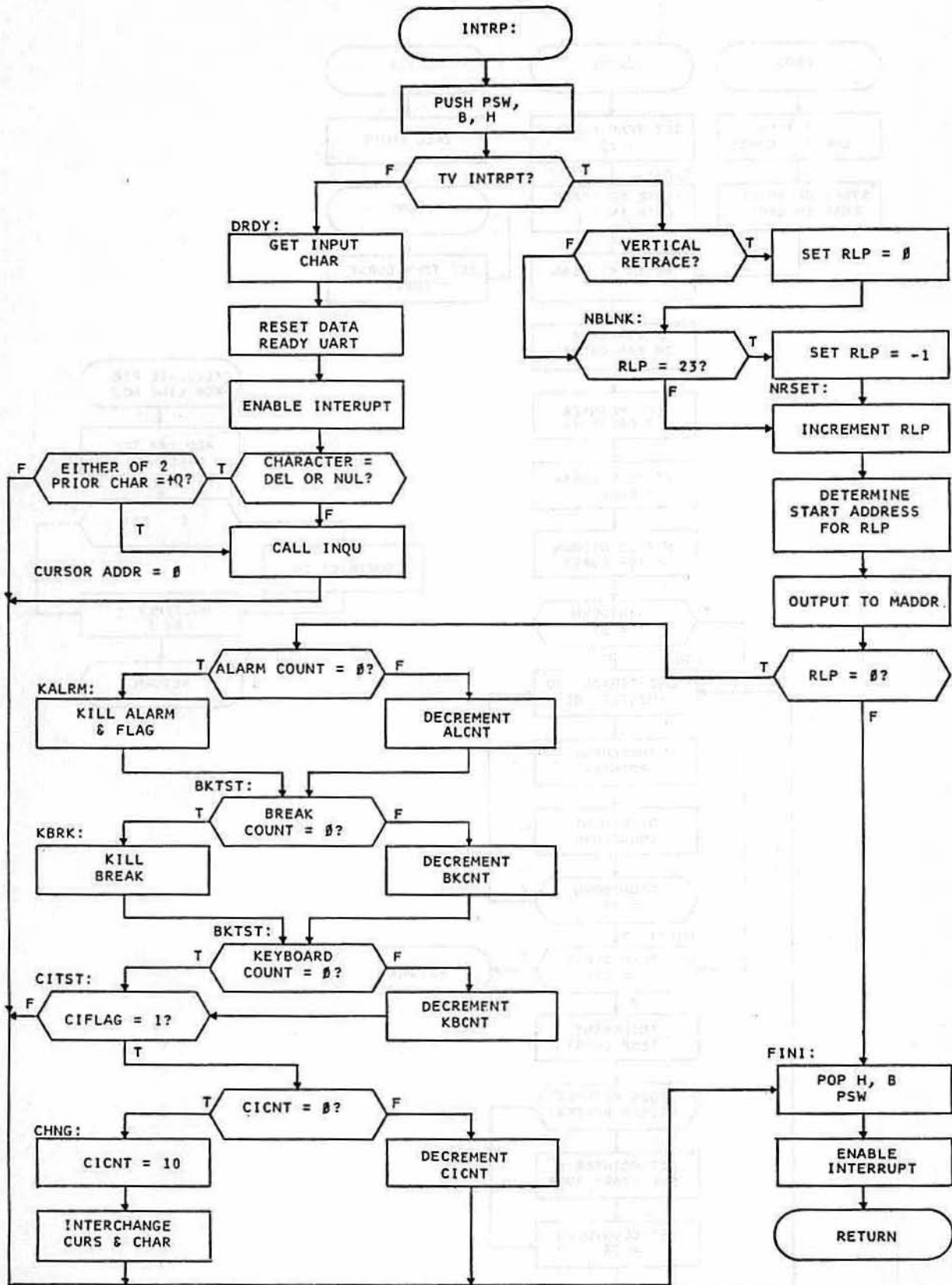
Filter



7784002

Figure 1-6. Flowcharts (Sheet 3 of 16)

Interrupt



7704054

Figure 1-6. Flowcharts (Sheet 5 of 16)

Clear Screen and Pointer

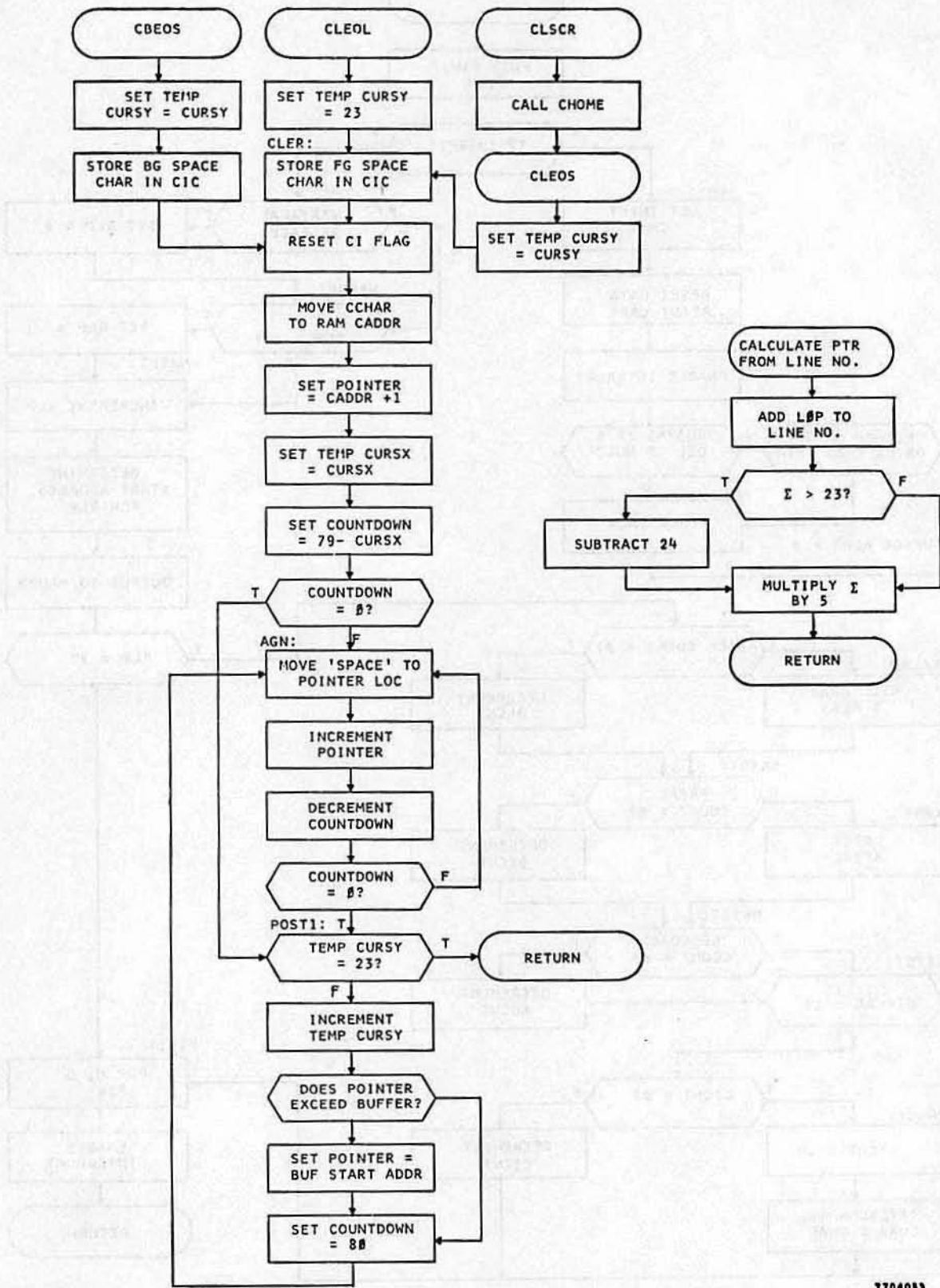
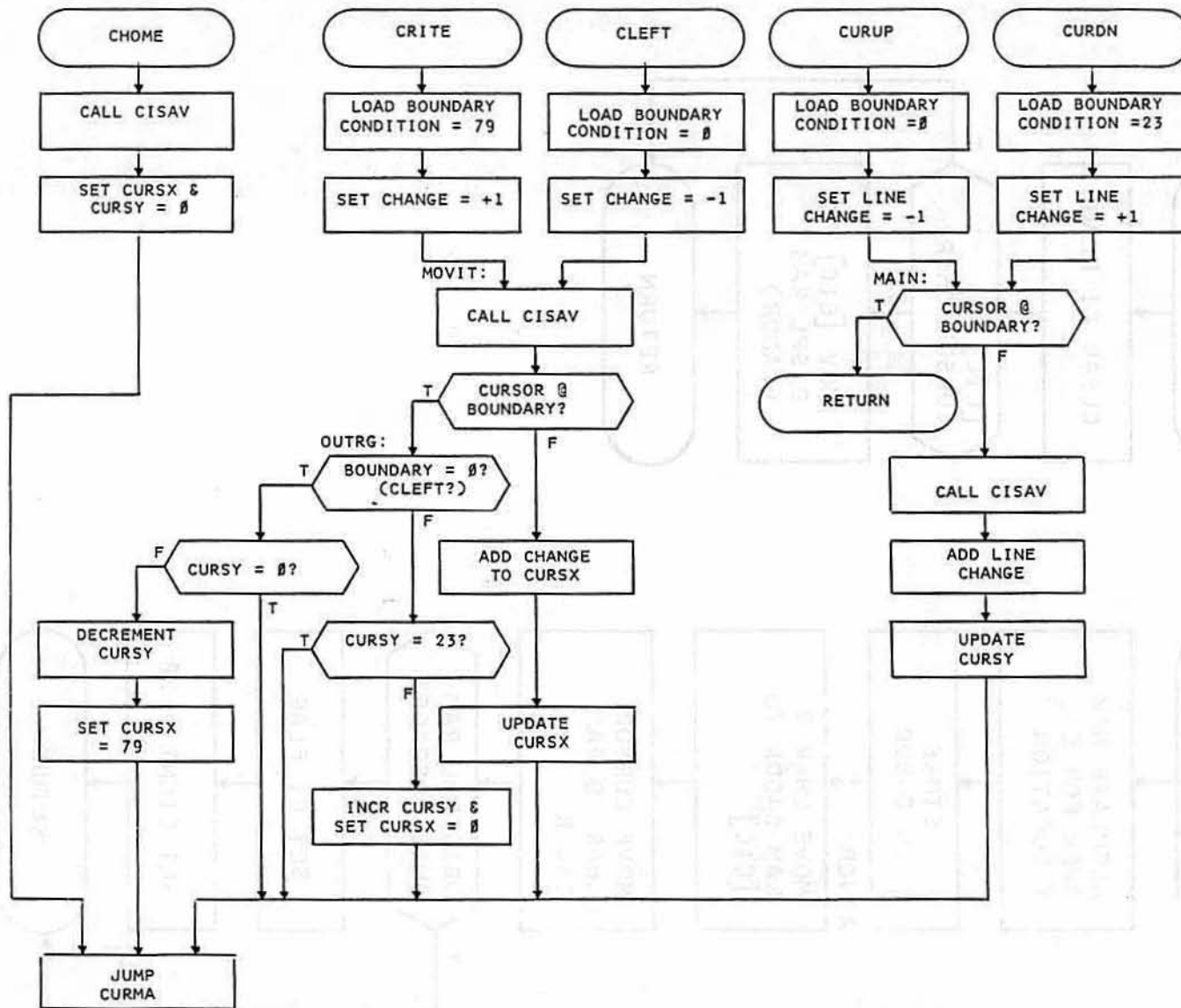


Figure 1-6. Flowcharts (Sheet 6 of 16)



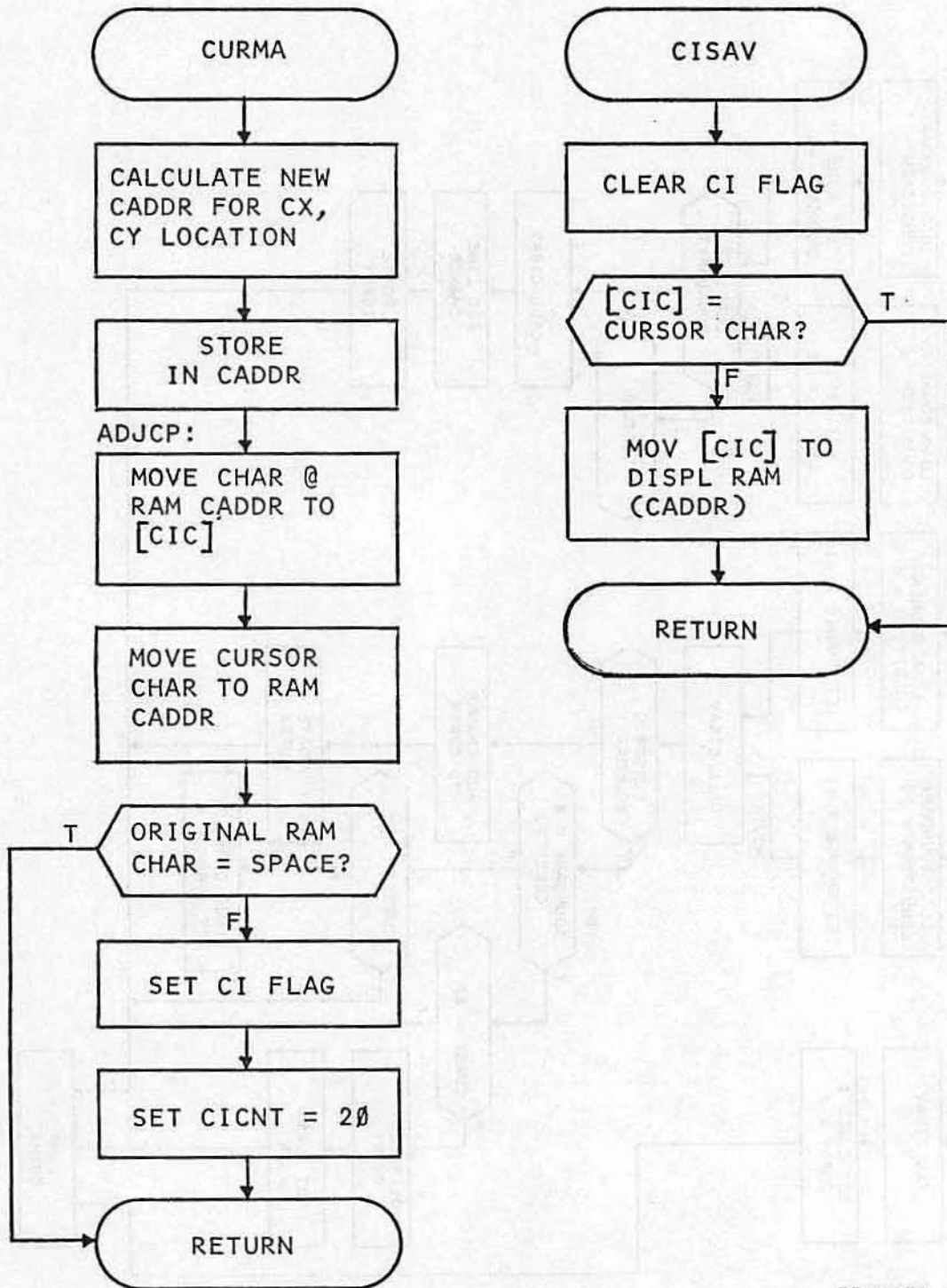
1-29

HI-1053A
Cursor Move

7704056

Figure 1-6. Flowcharts (Sheet 7 of 16)

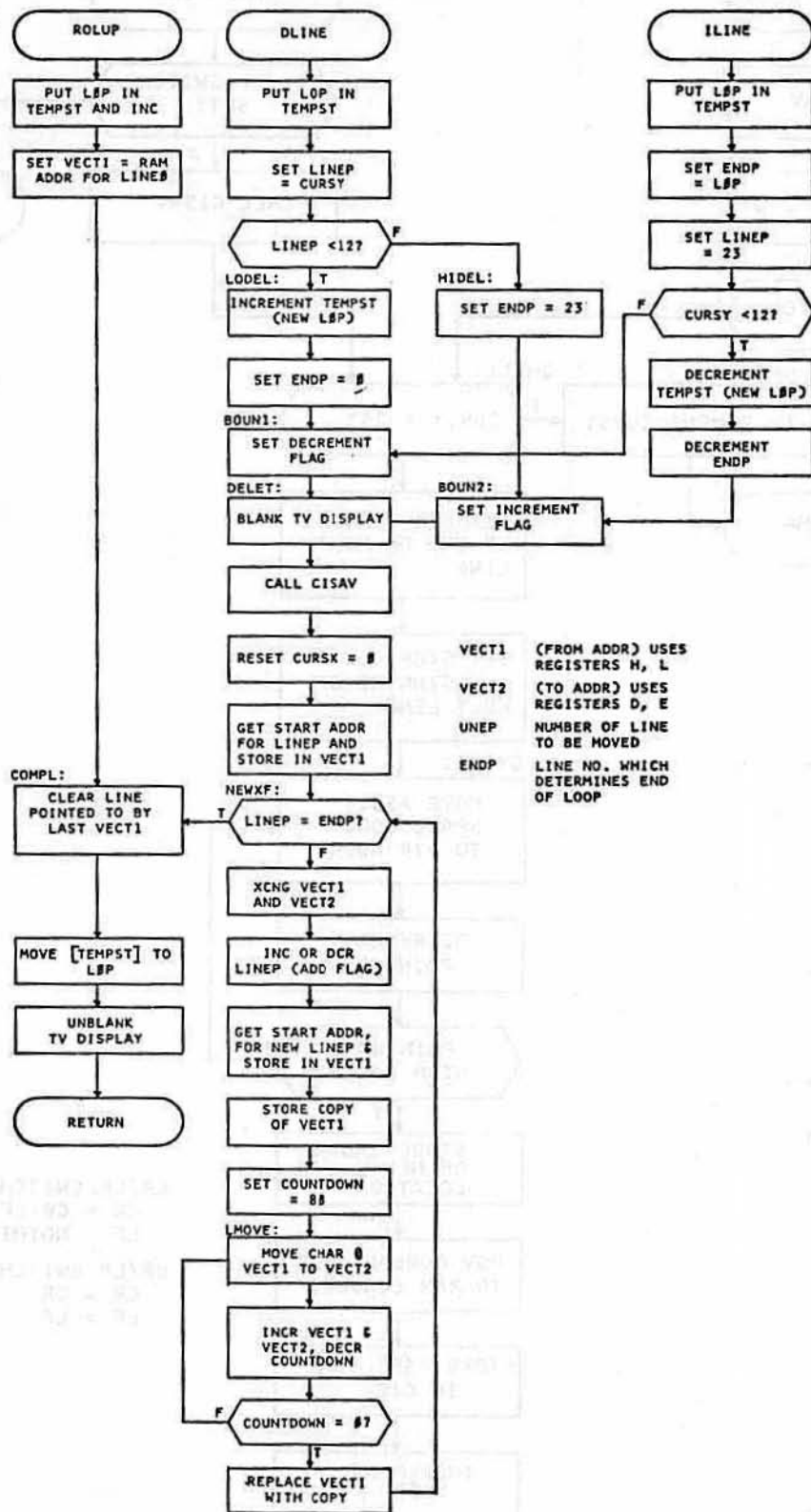
Cursor Interchange Save and Cursor Memory Adjust



7704057

Figure 1-6. Flowcharts (Sheet 8 of 16)

Rollup and Insert/Delete Line



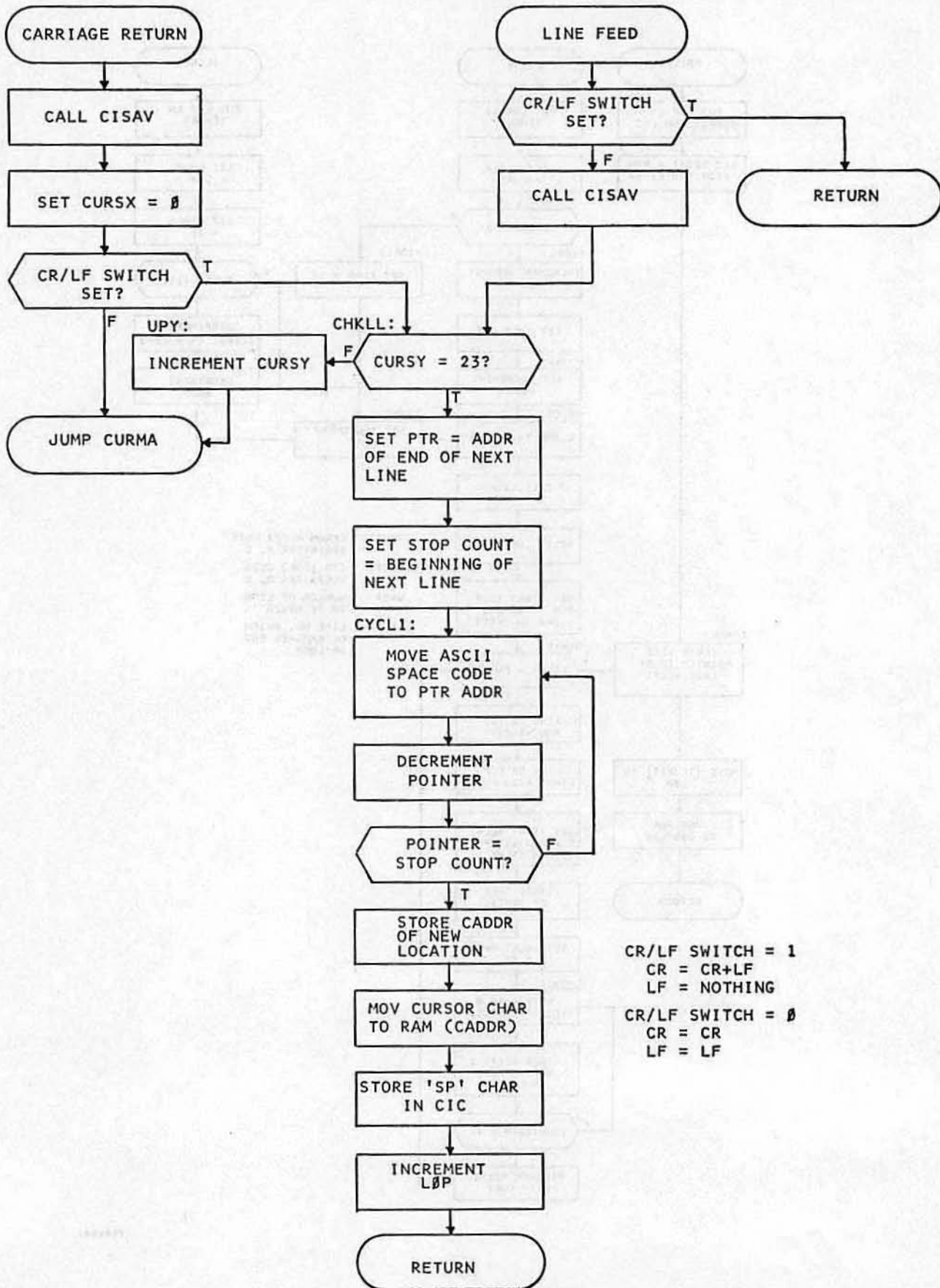
VECT1 (FROM ADDR) USES REGISTERS H, L
 VECT2 (TO ADDR) USES REGISTERS D, E
 UNEP NUMBER OF LINE TO BE MOVED
 ENDP LINE NO. WHICH DETERMINES END OF LOOP

7704043

Figure 1-6. Flowcharts (Sheet 9 of 16)

HI-1053A

Carriage Return/Line Feed

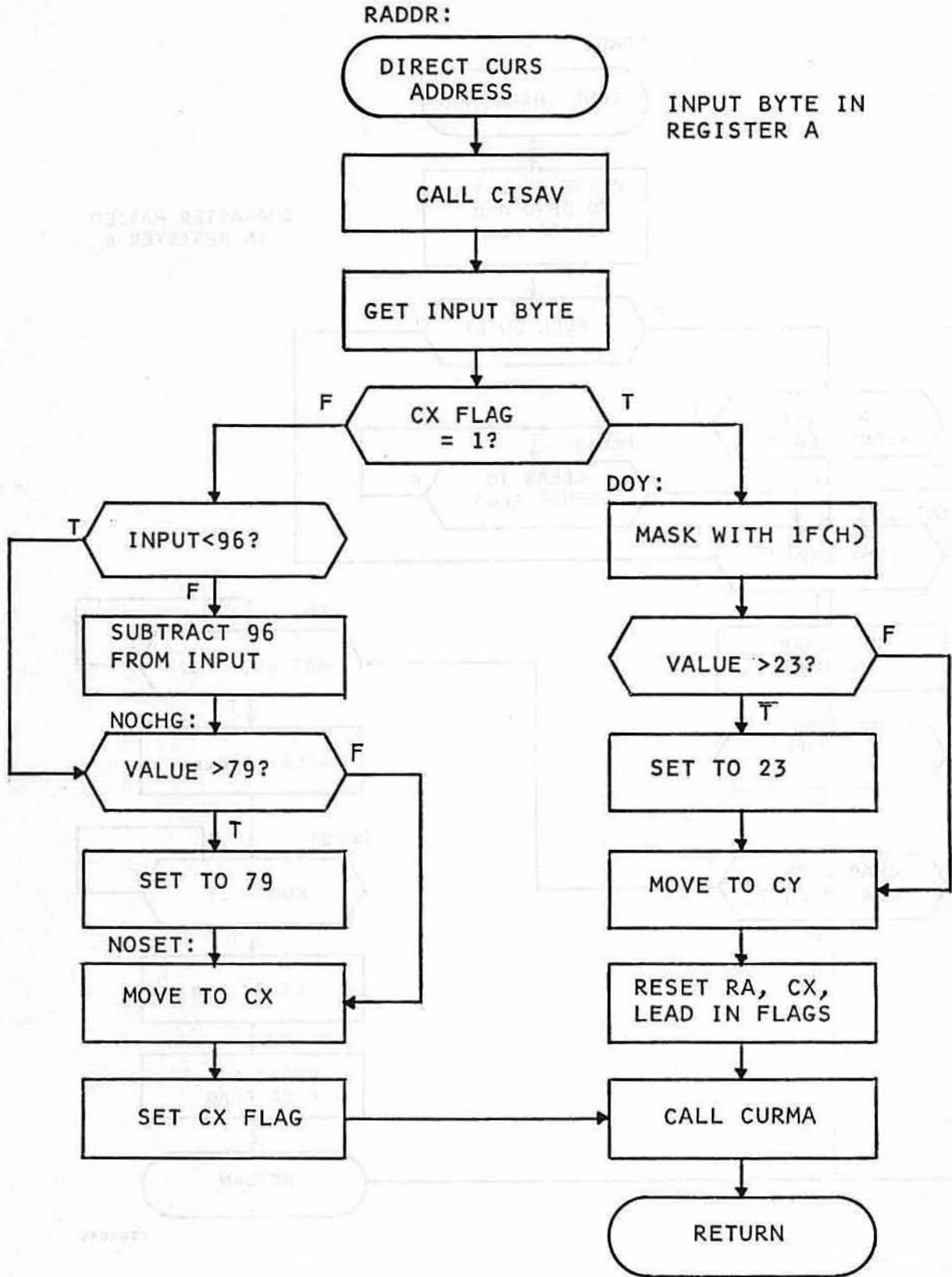


CR/LF SWITCH = 1
 CR = CR+LF
 LF = NOTHING
 CR/LF SWITCH = 0
 CR = CR
 LF = LF

Figure 1-6, Flowcharts (Sheet 10 of 16)

7704044

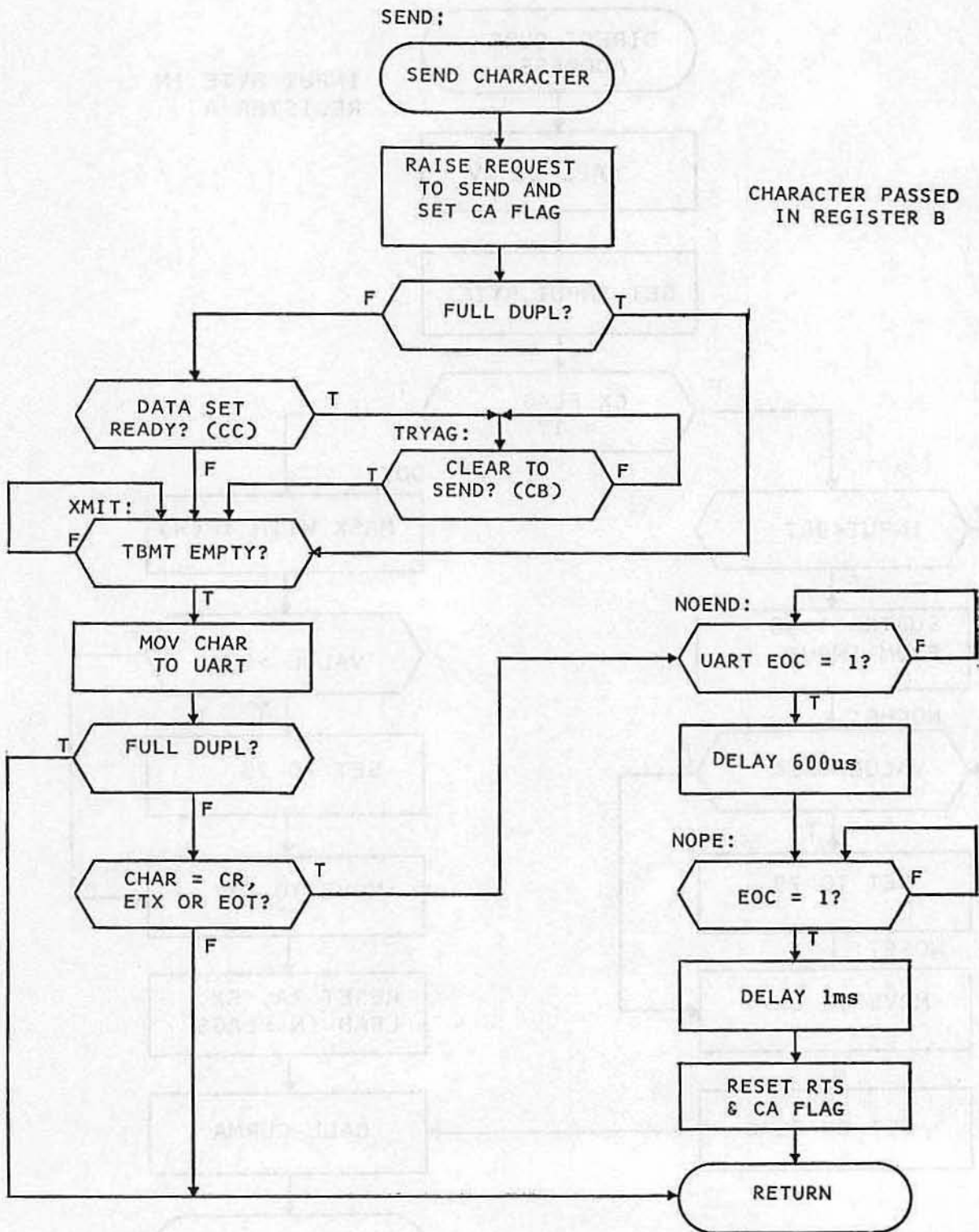
Direct Cursor Address



7704045

Figure 1-6. Flowcharts (Sheet 11 of 16)

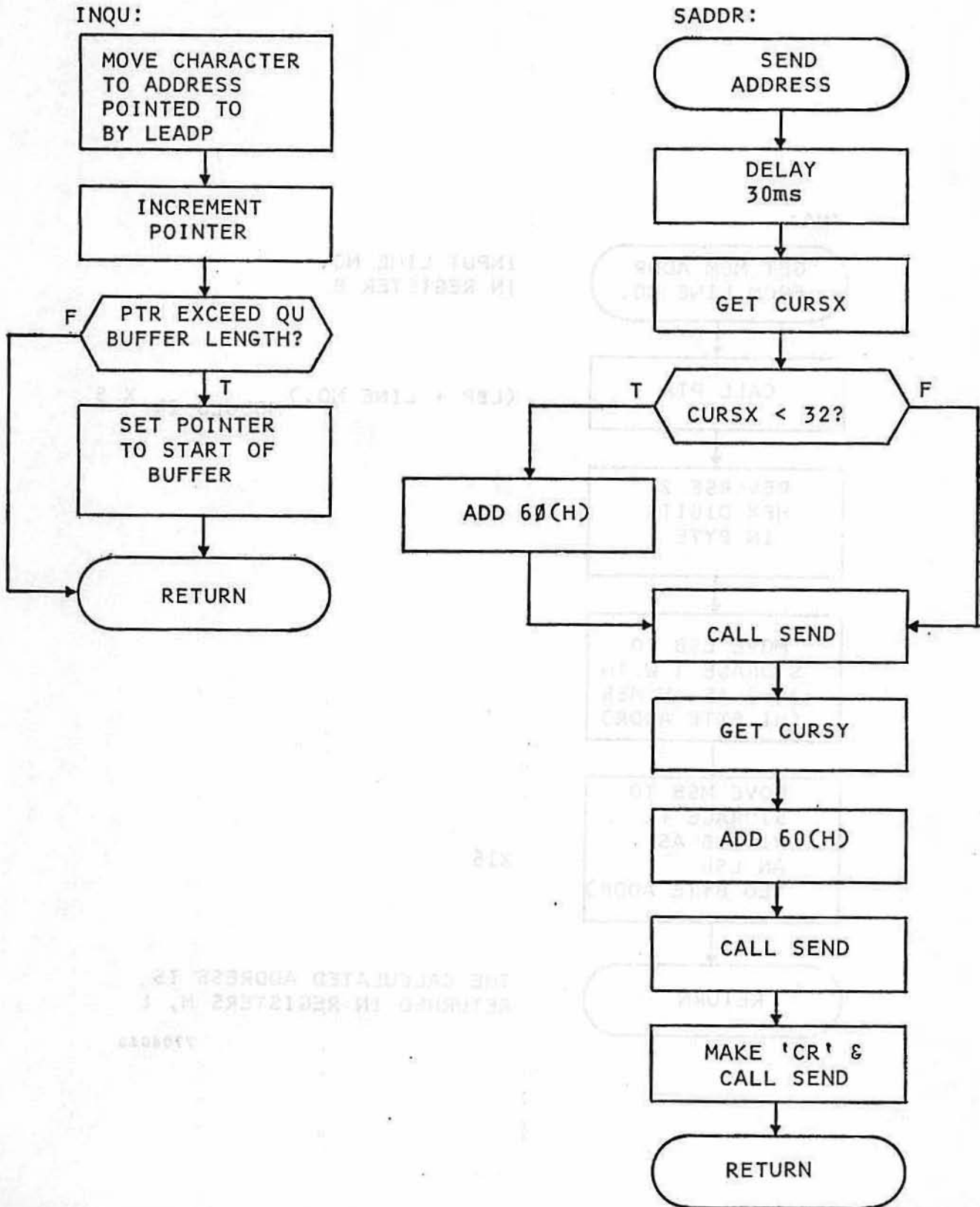
HI-1053A
Send Character



7704046

Figure 1-6. Flowcharts (Sheet 12 of 16)

Send Cursor Address and Queue

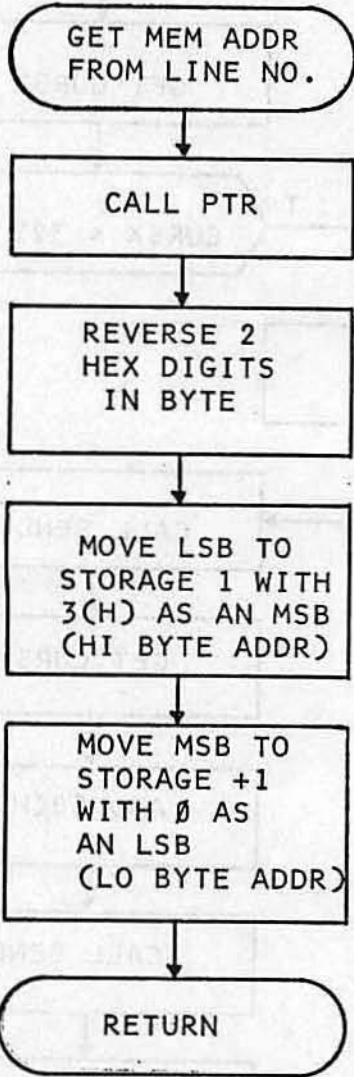


7704047

Figure 1-6. Flowcharts (Sheet 13 of 16)

Y Memory Address

YMA:



INPUT LINE NO.
IN REGISTER B

$(L0P + \text{LINE NO.}) \text{ MODULO } 24 \times 5$

X16

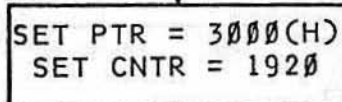
THE CALCULATED ADDRESS IS
RETURNED IN REGISTERS H, L

7704048

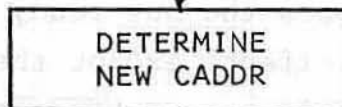
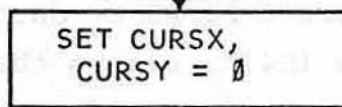
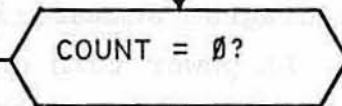
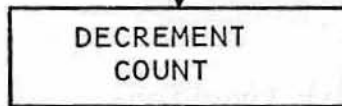
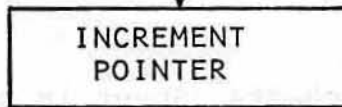
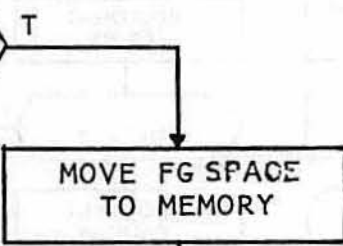
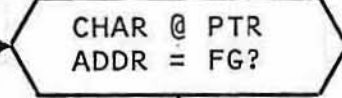
Figure 1-6. Flowcharts (Sheet 14 of 16)

Clear Foreground

CLFG:



DOAG:

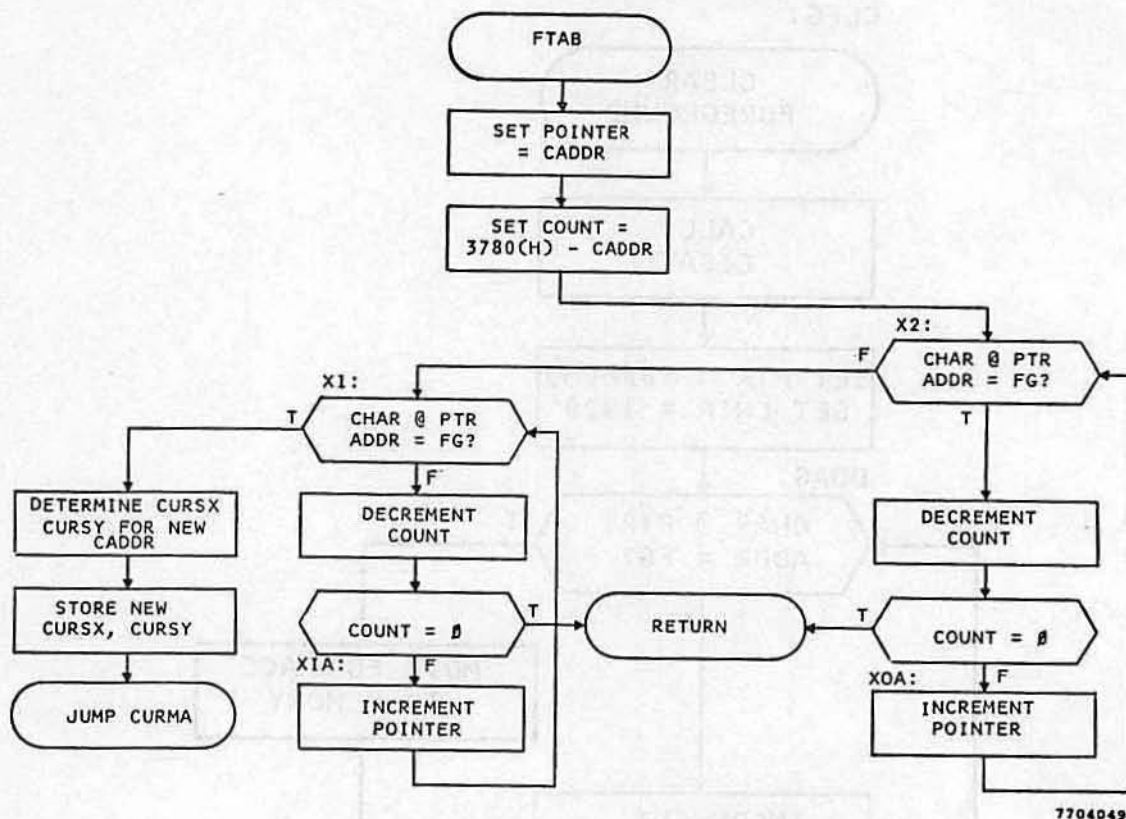


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Figure 1-6. Flowcharts (Sheet 15 of 16)

HI-1053A

Foreground Tab

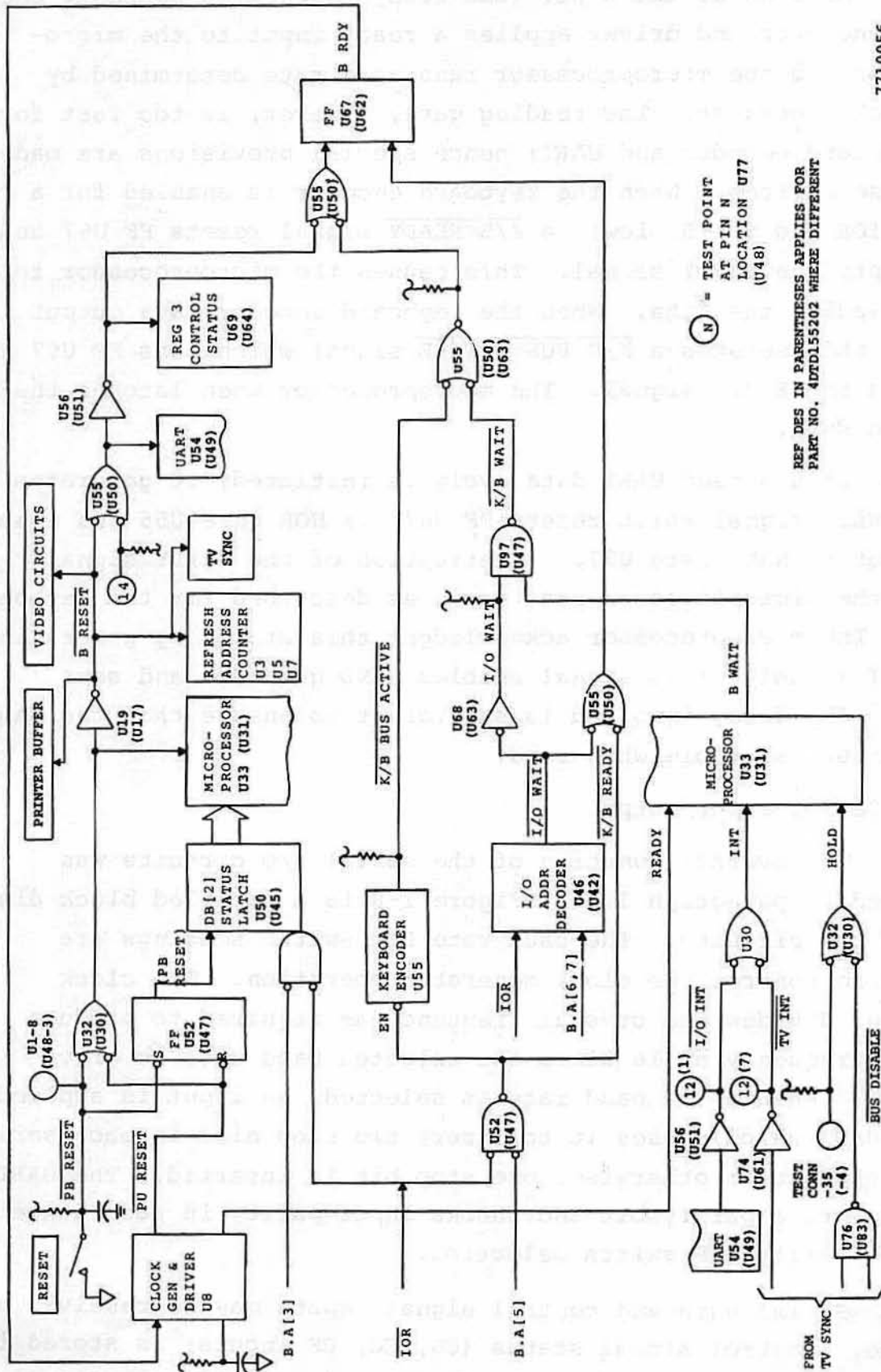


7704049

Figure 1-6. Flowcharts (Sheet 16 of 16)

1.3.5 Reset, Interrupt and Wait Functions

1.3.5.1 Figure 1-7 is a block diagram summarizing the reset, interrupt, and wait functions. At power turn on, the +5 volt supply charges a capacitor at an input pin of the clock generator and driver. This input triggers a $\overline{\text{PU RESET}}$ output which resets the pushbutton reset flip-flop (U47), resets the microprocessor, refresh address counter, printer buffer video circuits, UART, and control status register, and sets the bus ready flip-flop (U62). The RESET button has the same effect, except the pushbutton reset flip-flop is set. This status is transmitted to the microprocessor via the status latch, allowing the microprocessor to distinguish between a power up reset and a pushbutton reset (the screen is cleared for a power up reset but not for a pushbutton reset).



7710056

N = TEST POINT
AT PIN N
LOCATION U77
(U48)

REF DES IN PARENTHESES APPLIES FOR
PART NO. 40TDL55202 WHERE DIFFERENT

Figure 1-7. Reset, Interrupt, and Wait Functions, Block Diagram

1.3.5.2 As long as the B RDY (bus ready) signal is present, the clock generator and driver applies a ready input to the microprocessor and the microprocessor runs at a rate determined by the clock generator. The reading gate, however, is too fast for the keyboard encoder and UART; hence special provisions are made for these devices. When the keyboard encoder is enabled for a read cycle (IOR and B.A[5] low), a $\overline{K/B \text{ READY}}$ signal resets FF U67 and interrupts the B RDY signal. This causes the microprocessor to delay reading the data. When the keyboard encoder data output is stable, it generates a $\overline{K/B \text{ BUS ACTIVE}}$ signal which sets FF U67 and restores the B RDY signal. The microprocessor then latches the keyboard data.

1.3.5.3 When a read UART data cycle is initiated, it generates an I/O WAIT signal which resets FF U67 via NOR gate U55 and enables one input to NAND gate U97. Interruption of the B RDY signal delays the microprocessor read cycle as described for the keyboard above. The microprocessor acknowledges this status by generating a B WAIT signal. This signal enables NAND gate U97 and sets FF U67. The delay involved is sufficient to ensure that the UART data output is stable when read.

1.3.6 Serial Input/Output

1.3.6.1 The overall function of the serial I/O circuits was described in paragraph 1.3.1. Figure 1-8 is a detailed block diagram of the circuits. The baud rate DIP switch settings are decoded to control the clock generator operation. The clock generator divides the crystal frequency as required to produce a clock frequency at 16 times the selected baud rate to drive the UART. When a 110 baud rate is selected, an input is applied to the UART which causes it to insert two stop bits in each serial output character; otherwise, one stop bit is inserted. The UART also inserts a parity bit and checks input parity in accordance with the parity DIP switch selection.

1.3.6.2 Serial data and control signal inputs may be received at any time. Control signal status (CB, CC, CF inputs) is stored in status register 2. Data is stored in the input buffer and an I/O

interrupt signal is applied to the microprocessor whenever a character is received.

1.3.6.3 The remaining functions are controlled by the microprocessor via the local address decoder. By the appropriate control and address bits, the microprocessor can command any one of four operations as follows:

<u>Operation</u>	<u>Function</u>
Read data	Causes the received data in the UART input buffer to be transferred to the microprocessor (along with a parity error bit if an error is detected) and causes an I/O wait as described in paragraph 1.3.5.3.
Write data	Causes data from the microprocessor to be transferred to the UART transmit buffer from which it is automatically sent as serial output.
Read status	Transfers the contents of status register 2 (and the UART end-of-character bit) to the microprocessor.
Write status	Updates status register 3.

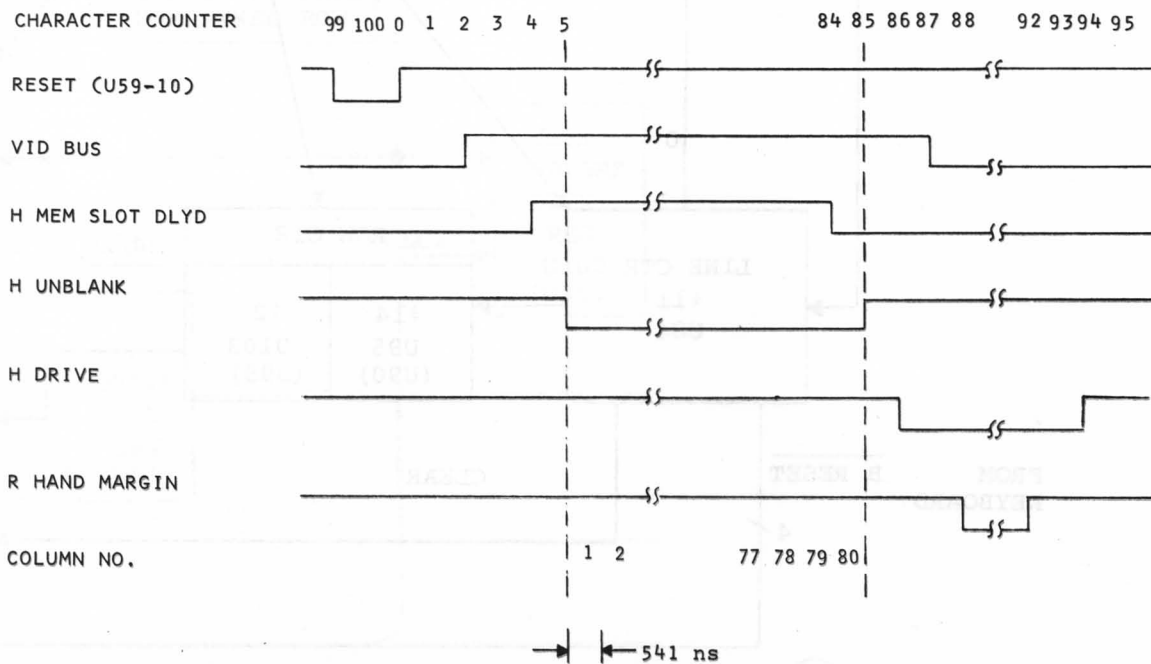
1.3.6.4 When input data is read, the microprocessor transmits a data ready reset bit to register 3, which clears the UART input buffer. Register 3 also stores the control outputs (request to send and data ready), the break, and the alarm (BEL) controls.

1.3.7 TV Synchronizer

1.3.7.1 The overall function of the TV sync circuits was described in paragraph 1.3.1. Figure 1-9 is a detailed block diagram of the circuits. The horizontal circuits are shown on the top half of the diagram. The 33.264 MHz oscillator and divide-by-two flip-flop generate the 16.632 MHz video clock. This is the dot frequency (one pulse for each of the nine horizontal resolution elements of each character (figure 1-5)). The divide-by-nine shift

register outputs are decoded by the dot count register to produce dot, Ndot and line buffer clock outputs during selected portions of each character window. A character counter output selects addresses in the horizontal sync prom, and the decoded prom outputs are the basic horizontal sync signals. The timing is shown in figure 1-10.

1.3.7.2 The right hand margin outputs of the horizontal section are counted by the vertical section to generate the vertical sync signals. A divide-by-eleven counter counts the eleven lines in each character window. An output at line 10 of each 11-line character row enables the bus disable signal (which puts the microprocessor in the hold condition and enables the refresh address counter output), and the CNT CLK signal (which is the clocking signal for the refresh address counter). This synchronizes transfer of a new row of characters from the display memory to the video line buffers. The line count ($LC2^0 \sim LC2^3$) is also used by the video line buffers to load a new input on line 10, and to recirculate data on lines 0 through 10.



7704041

Figure 1-10. Horizontal Timing

1.3.7.3 The line counter output is divided by 28 and decoded to form the vertical sync signals. Timing is shown in figure 1-11.

1.3.8 Microprocessor

1.3.8.1 Figure 1-12 is a block diagram of the microprocessor circuits. Basic $\phi 1$ and $\phi 2$ clocks are generated by the clock generator to drive the microprocessor chip. These clock pulses occur at a 2 MHz rate and a nominal 10 volts (9.4 volts minimum). The clock generator also generates a power-up reset signal, triggered by the charging of an external capacitor, and synchronizes the bus ready signal to the microprocessor.

1.3.8.2 During the first part of a processor cycle, synchronous with the \overline{STSTB} (status strobe) signal, a status word appears on the microprocessor data bus. This indicates the type of cycle to be performed and is stored in the system controller status latch. Depending on the type of operation to be performed, the gating

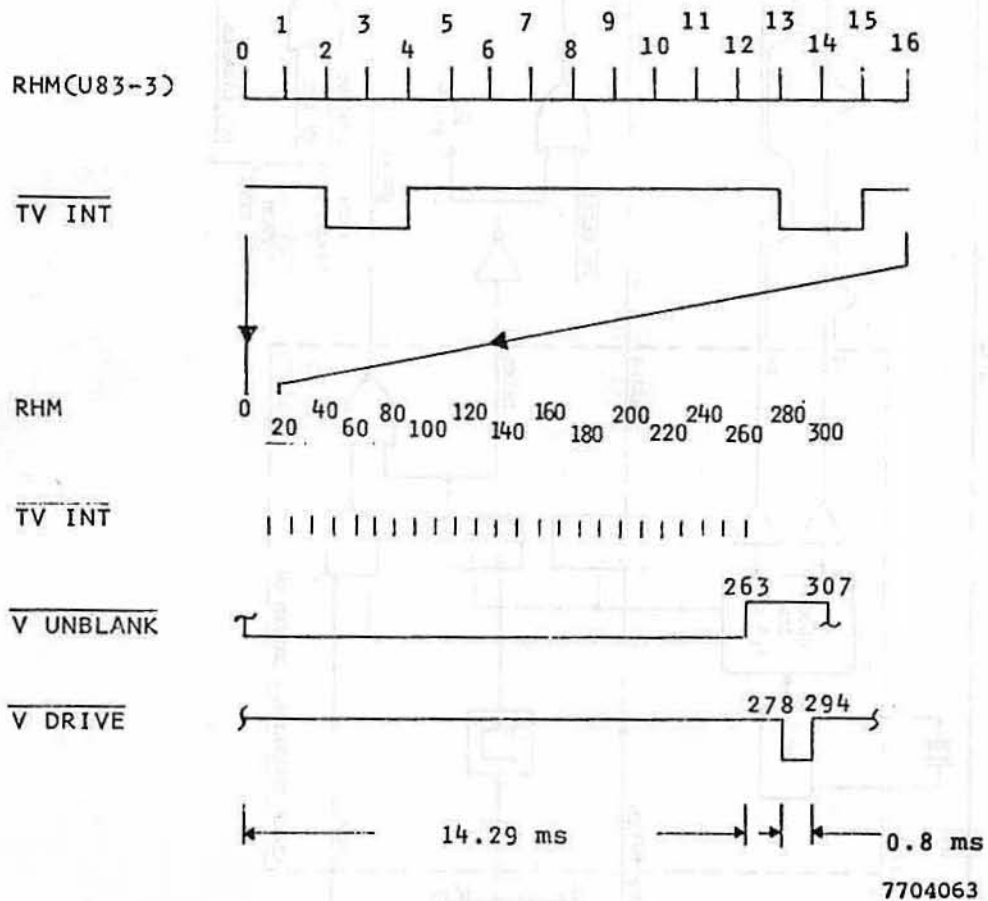


Figure 1-11. Vertical Timing

array generates a memory write or I/O write output synchronous with the microprocessor WR (write) signal, or a memory read or I/O read signal synchronous with the microprocessor DBIN (data bus input) signal. The gating array also controls the direction of the bus drivers and generates an $\overline{\text{INTA}}$ (interrupt acknowledge) signal when the microprocessor status word indicates an interrupt. The interrupt occurs in response to an external interrupt input to the microprocessor.

1.3.8.3 A bus disable input to the microprocessor causes it to go into the hold condition. The microprocessor then generates a HLDA (hold acknowledge) signal which is also used as a bus enable/disable control. The address and data bus drivers are 3-state devices. During the hold status, they are in the high impedance state, permitting other devices to control the address and data buses. This feature, called direct memory access, is used during tv refresh to permit direct transfer from refresh memory to the line buffer.

1.3.9 Monitor (Figure B-4)

1.3.9.1 Low-Voltage Regulator. The low-voltage regulator processes input ac power, converts it to a highly regulated dc voltage, and supplies this voltage to all circuitry in the monitor. The regulator output voltage also determines the raster width for the crt display. Primary ac power (98 vac, 60 Hz, nominal) is received from a secondary winding in the power transformer. This voltage is rectified by U3, filtered by C26A, and subsequently regulated by the circuitry described below.

1.3.9.1.1 The regulator circuit is a closed loop feedback amplifier, with high open loop gain for stability, and current amplification to provide adequate power to drive the remaining monitor electronics. A reference voltage is established by resistor R55 and zener diode VR3 at the high impedance port of operational amplifier U2. Because of the large open loop gain of U2, this same voltage is reflected, by means of a virtual ground between pins 2 and 3 of U2, at pin 3 of U2. Feedback network R56, R57,

and R58 then determine the magnitude of the regulated voltage (amplifier gain) at the emitter of output transistor Q7.

1.3.9.1.2 Amplifier U2 and transistor Q9 provide open loop voltage gain and voltage translation of the input reference voltage. Transistors Q7 and Q8, connected as a Darlington amplifier, provide current and power gain for delivery to the monitor circuitry. Resistors R51 and R52 provide bias for amplifier U2. Resistors R49 and R50 provide bias for the transistors. Resistor R54 provides emitter degeneration for the Darlington. Capacitor C27 provides frequency compensation for amplifier stability and capacitor C26B provides dynamic load filtering for the regulated output.

1.3.9.1.3 Dynamic operation of this amplifier is as follows. An instantaneous increase of the output voltage increases the voltage at the arm of potentiometer R57. The difference between this voltage and the reference voltage at pin 2 of U2 is amplified by difference amplifier U2 whose output then increases base drive and collector current in transistor Q9. This increase in current then tends to starve, or turn-off, transistors Q8 and Q9. Therefore, the emitter current of Q7 decreases which, in turn, tends to decrease the output voltage such that stable circuit operation for varying circuit loads is maintained.

1.3.9.1.4 Potentiometer R57 permits adjustment of the output voltage and is used to establish correct raster width on the crt display. Fuse F2 provides protection in case of fault or failure conditions in the monitor electronics.

1.3.9.2 Video Amplifier. The video signal originates in the logic, is routed through an operator-controlled contrast potentiometer, and enters the monitor on pin 8 of the monitor input connector P1 with a ground return reference at pin 5 of P1. The video signal is terminated on the pc board by R75 and is then processed by transistors Q10 and Q11 connected as a cascode amplifier with a nominal dc gain of 25, controlled by resistors R65, R66, and R67. Capacitor C30 provides high frequency peaking of the video signal to permit a uniform brightness presentation on the crt of both single dots and horizontal bars within an alphanumeric

character. The output video signal at the collector of transistor Q10 is coupled to the crt cathode through inductor L5 and through resistor R69 which is located in the crt socket assembly. L5 provides further peaking of the signal; R69 provides crt flashover protection for the video amplifier circuitry. A spark gap at the socket provides further flashover protection. Resistor R64 and capacitor C29 provide decoupling of the B+ line. Resistors R63 and R74, capacitor C28, and Zener diode VR5 provide base drive and a low source impedance for the upper transistor of the cascode.

1.3.9.3 Horizontal Deflection. The horizontal deflection amplifier provides deflection yoke drive to move the crt electron beam across the screen. The deflection is a closed loop system consisting of an AFC circuit and drive output stage. The system is closed because the output (flyback pulse) is fed back to the AFC circuit for phase comparison with the incoming synchronization pulses.

1.3.9.3.1 The AFC circuit portion of the horizontal deflection comprises Q13, U2 and their associated components. The sync from the logic board is TTL, positive-going. Q13 is used to invert the sync since U2 requires a TTL negative-going input at pin 3. Q13 also serves as a buffer between the deflection and the logic board. U2 contains a regulator, phase comparator, voltage-controlled oscillator, and an output pulse width controller. The internal regulator voltage is measured at pin 6 of U2 (8.6 V nominal) and provides oscillator stability during environmental change, power supply drift, and component tolerance drift. The voltage-controlled oscillator is set nominally by adjustment of R5. R5, in conjunction with R6, R7, R8 and C1, determines the oscillator's free-running frequency (no sync input). The filter, composed of R9, R12, C2 and C3, filters the voltage that controls the oscillator. The amplitude of the control voltage is proportional to the difference in phase of the feedback signal (flyback in this case) and the input sync. The flyback pulse is integrated by R13 and C6 to produce a sweep at the horizontal rate. C5 ac-couples the sweep into the phase detector for comparison against the incoming sync.

The output pulse width at pin 1 of U2 is determined by the ratio of R10 and R11. The pulse is routed to Q1 to drive the primary of pulse transformer T2. The secondary of T2 supplies base drive for Q2, the horizontal output transistor.

1.3.9.3.2 The output stage is a flyback deflection system. The description starts at the time the sweep has reached the right portion of the crt and is ready for flyback initiation. Q2 is conducting at this time and the yoke current is sweeping negatively. The sync pulse (already described), coupled by T2, turns Q2 off. The yoke, which no longer has a discharge path, now dumps it's energy into flyback capacitor C11. The yoke and C11 act as a tank circuit and ring at the frequency determined by their values. The ring causes the voltage at Q2 collector to increase to approximately 600 V. When the voltage returns to ground potential and attempts to ring negatively, diode CR1 turn on to clamp the negative excursions. At this point, the yoke current has again returned to its positive extreme (left side of crt) and the sweep starts again. Approximately half way through the sweep, Q2 turns on again, CR1 turns off and the sweep continues until the sync pulse initiates flyback again. Coil L2 is used to compensate for losses in the yoke. C12 and R18 damp any spurious ringing within L2. C31 is the "S" correction capacitor and compensates for geometrical non-linearities caused by crt face-place curvature. Power for the system is supplied by the 70 V regulator via the flyback transformer, T3. Adjustment of the regulator voltage controls the width of the horizontal sweep. Increasing the voltage increases the size of the sweep.

1.3.9.4 CRT Electrode Drives. All crt electrode potentials (except video) are derived from the horizontal deflection flyback voltage, as follows.

a. CRT Anode Voltage. The horizontal pulse at the collector of Q2 is applied to the primary of the flyback transformer (pin 5 of T3). This pulse is stepped up, through transformer action, to a magnitude of 15,000 volts, is then rectified by CR4 and applied to the crt anode.

b. DC Focus Voltage. The horizontal pulse at the collector of Q2 is rectified by diode CR2 and applied to one end of focus potentiometer R22. The horizontal pulse is also ac-coupled and rectified by C14 and CR3 and applied to the other end of R22. The wiper voltage of R22 is then applied, through R21, to the crt focus electrode. This circuitry establishes the dc focus voltage for the crt and can be varied from approximately -400 volts to +500 volts to achieve optimum focus.

c. Dynamic Focus. A tapped voltage from the primary of T3 is ac-coupled and resonated by action of L3 and C17. A sinusoidal voltage at the horizontal frequency is developed at C17 and the voltage phase and amplitude is controlled by varying L3. This ac voltage is summed with the dc focus voltage to produce a composite focus potential to optimize focus over the entire crt display.

d. G2 Voltage. This voltage is developed in a fashion similar to the dc focus voltage. The horizontal flyback pulse is rectified by CR3, filtered by R23, C16, and R24, and applied to the second crt grid.

e. G1 Voltage. The voltage applied to this first (control) crt grid is used to control raster background brightness. Voltage is applied to both ends of brightness potentiometer R26 and is limited in value by resistors R25 and R27, such that the total G1 voltage range is from approximately -90 volts to +30 volts. A vertical blanking signal is also coupled into this electrode. The vertical blanking signal is discussed in paragraph 1.3.9.5.

f. Filaments. A primary tap on flyback transformer, T3, is used to drive the crt filament electrodes. The voltage developed is 6.3 vac.

g. Spark Gaps. Each electrode discussed in paragraphs b. through f. above has a series swamping resistor separating it from its drive circuit. Each of these electrodes also has a spark gap returned to ground. The purpose of these spark gaps and

resistors is to divert and limit occasional crt flashover energy, thereby preventing monitor failures.

1.3.9.5 Vertical Deflection. The vertical deflection supplies the yoke with the necessary current to drive the crt electron beam from the top to the bottom of the display. Q14 and Q3 provide the vertical integrator with the proper sync signal and also with the capability to free-run (no sync applied). Q14 provides buffering between the deflection circuit and the logic board and also translates the sync level to a value that is usable by Q3. Q3 is programmable unijunction transistor. Q3 remains in a non-conductive state until the voltage on its gate (connected to R32) is exceeded by the voltage on its anode (connected to R37). When the anode voltage exceeds the gate voltage, Q3 turns on and conduct from anode to cathode. The voltage at the anode is controlled by the charging of C19 and C32 through R37 and R36 (R36 is a positive temperature coefficient resistor). This charging waveform is the sweep generating waveform. As the sweep reaches a predetermined value, adjustable by R36 (vertical height control) the sync pulse at the gate causes the gate voltage to drop below the anode voltage. Q3 turns on, thereby discharging C19 and C32 to the level determined by CR6 and CR7. Q3 runs off and the cycle begins again.

1.3.9.5.1 In the case where sync is absent, the level at Q3 gate is determined by R31 and R33. The anode sweep waveform charges to this value, Q3 turns on as defined previously, and the system oscillates independently.

1.3.9.5.2 The sweep waveform generated by R36, R37, C19 and C32 is applied to the base of Q4. Darlington transistor Q4 drives the vertical output transistor, Q5, and the linearity correction network, consisting of R38, C20, R39 and R40. The linearity correction network feeds a portion of the output waveform determined by R39, linearity control, back to the junction of C19 and C32. Resistor elements in this network are high stability film resistors. This signal causes the generated sweep to assume the

characteristic "S" shape and corrects for non-linearity caused by crt screen geometry.

1.3.9.5.3 The output transistor Q5 provides the necessary current amplification to drive the yoke. C22 couples the sweep to the yoke and ensures that the sweep is centered around ground potential. L4 provides the necessary current required to drive the output system. R44 and VDR-1 damp the flyback voltage created when the vertical sweep retraces. VR2, R43, and R83 supply the low voltage/current section with the dc power required for their operation.

1.3.9.5.4 The blanking signal is derived by using the vertical flyback at Q5 collector to turn Q6 on. R47 and R48 determine the amplitude of the blanking pulse. C24 ac-couples the blanking pulses to the control grid where they are summed with a dc potential supplied by R25, R26, R27 and R81. R26 is used to adjust the level of the voltage at the blanking grid and thereby adjusts display brightness.

1.3.10 Five-Volt Regulator (Figure B-3)

1.3.10.1 The 11-volt ac input from the power transformer is rectified by CR3 to supply the regulator circuits. Power for regulator integrated circuit A1, filtered by C1 and R1, is applied to pins 7 and 8. The regulator integrated circuit generates a 7.15 volt reference voltage at pin 4. A fraction of this voltage, divided by R10 and R11, is applied to pin 3 as the reference level (approx 4.2 vdc) for voltage comparison. A fraction of the output voltage at terminal 4, divided by R8 and R9, is applied to V1 pin 2. The voltages at pins 2 and 3 are compared to determine the output at pin 6. If the voltage at pin 2 increases, the output at pin 6 is reduced, reducing the conduction through series transistors Q1 and Q4 and reducing the output voltage. If the voltage at pin 2 decreases, the output at pin 6 increases, raising the output voltage. R6 and C3 provide frequency compensation for the regulator integrated circuit.

1.3.10.2 If the output current from the regulator increases, the base voltage at Q1 and Q4 rises in order to maintain the output

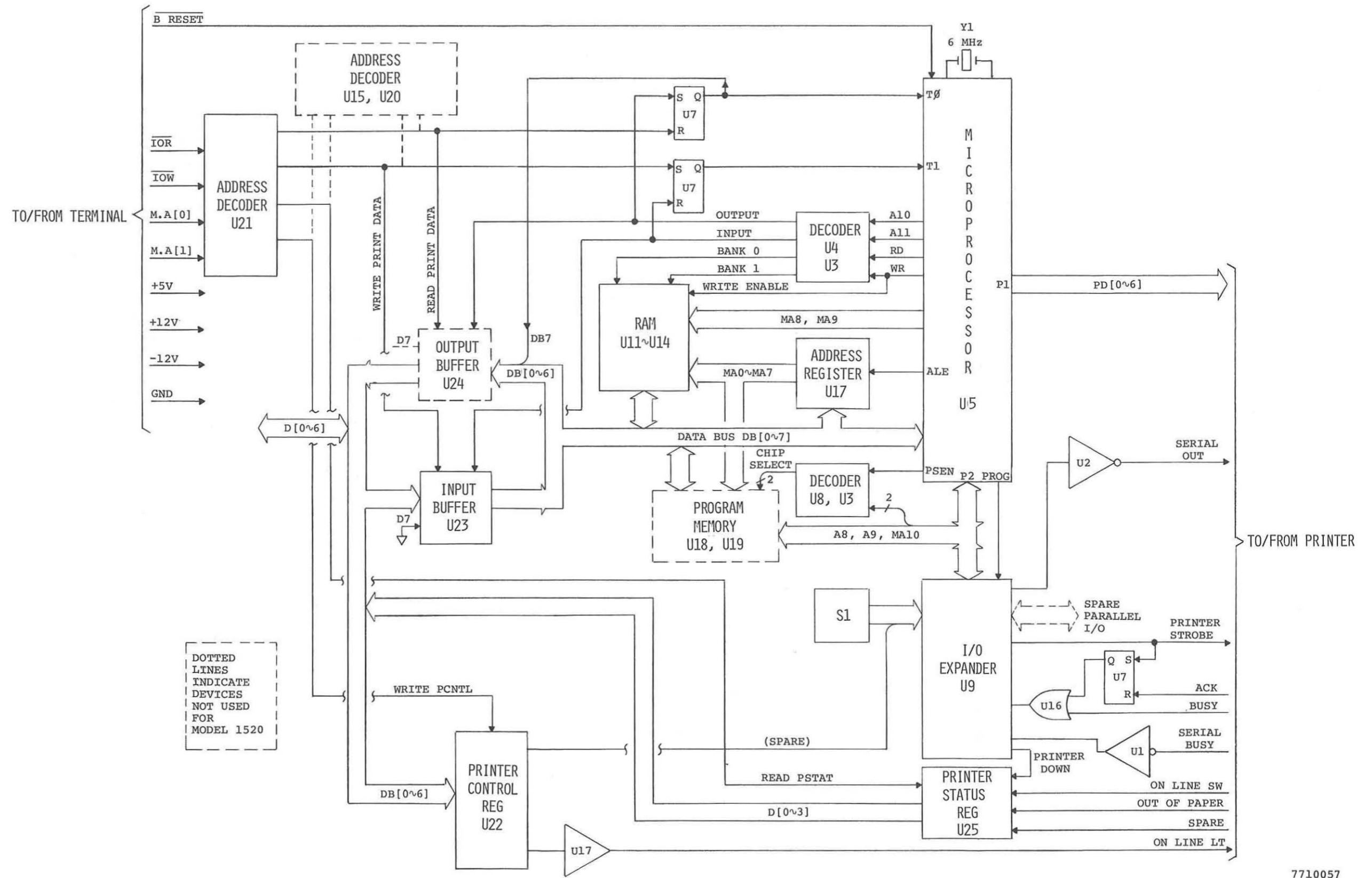
voltage. A fraction of the base voltages developed across R3 is applied to A1 pin 10 via R4 and R19. Potentiometer R19 is adjusted so that the current limit feature of A1 is triggered when the output current exceeds normal by 20 percent. The output at A1 pin 6 is then lowered, reducing the output current of the regulator.

1.3.10.3 Q2 and Q3 provide overvoltage protection. If the regulator output voltage rises, the full increase appears at the emitter of Q2. Only a fraction of the increase appears at the base of Q2. Potentiometer R18 is adjusted so that Q2 conducts sufficiently to trigger the gate of Q3 if the output voltage reaches +6 vdc. Q3 then conducts, cutting off the output.

1.3.11 Printer Buffer (Figure 1-13)

1.3.11.1 The printer buffer includes a 2048 word random access memory and a microprocessor to buffer and control transfer of data to a printer in parallel or serial format. The microprocessor has an I/O expander which is used to increase the number of input/output ports available to the processor. Under control of the P2 and PROG (program) signals, parallel words can be transferred via the remaining four ports of the expander. The microprocessor in the printer buffer handles addressing differently than the one in the terminal logic. The least significant eight bits are output on the data bus, along with an ALE (address latch enable), and are held in the address register. The most significant bits are then output with a read or write command. The processor program is stored in ROM on the microprocessor chip.

1.3.11.2 Data is transferred between the terminal and printer buffer under control of the two microprocessors as follows: Data to the printer buffer is put on the terminal data bus D[0~6] along with a write command which the address decoder translates to a write print data command. This command gates the data into the input buffer and sets a flip-flop, which generates a T1 input to the microprocessor, denoting data present in the input buffer. The printer buffer microprocessor, in turn, generates the appropriate commands to transfer the word on the printer buffer data



7710057

Figure 1-13. Printer Buffer, Block Diagram

bus, and reset the flip-flop. The terminal may also read printer status from the printer status register or transfer a control word to the printer control register via the terminal data bus.

1.3.11.3 Parallel output to the printer is directly from the microprocessor at TTL levels, accompanied by a printer strobe. The strobe sets a flip-flop which inhibits further transmission until an ACK (acknowledge) from the printer resets the flip-flop. Timing is shown in figure 1-14. A busy signal from the printer will also inhibit transmission, and if it persists for 6 seconds the microprocessor does not send a "buffer empty" bit via the printer status register. Parallel operation is selected by switch S1-1,2,3 (a dip switch on the circuit board). The rate of transmission is determined by the availability of data in the buffer and the rate at which it is acknowledged by the printer.

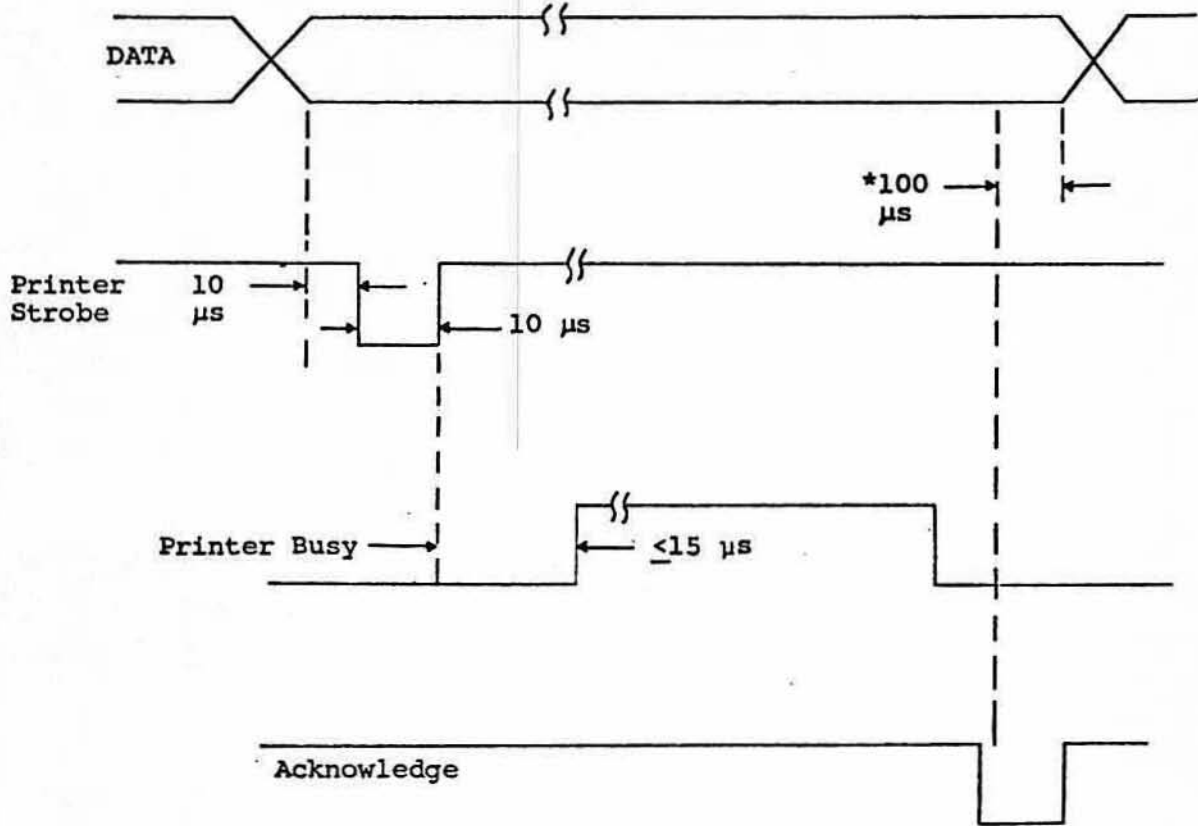
1.3.11.4 Serial output to the printer is transmitted via a TTL to EIA level buffer at a rate of 110, 300 or 1200 baud, selected by S1-3 and S1-1,2. Timing is accomplished by a timer in the microprocessor. Transmission is inhibited if the serial busy signal from the printer is present.

1.3.11.5 The following capabilities of the printer buffer are not used in the model 1520:

- A seven bit parallel input output port is available at the I/O expander.

- An external program memory for the microprocessor.

- An output buffer for transferring data to the terminal data bus.



*If Acknowledge is grounded, data access is initiated from drop in Printer Busy.

Figure 1-14. Parallel Printer Interface Timing

SECTION 2

SITE MAINTENANCE

2.1 INTRODUCTION

2.1.1 Scope

This Section provides troubleshooting, adjustment and replacement procedures for servicing terminals at the user's site. Recommended spares are listed in Appendix A.

2.1.2 Test Equipment

A standard Hazeltine serviceman's kit containing the following items is recommended for site maintenance.

Hand tools

Alignment tools

Volt-Ohmmeter, digital

Spare parts allocation (refer to Appendix A)

2.2 CHECKOUT

2.2.1 General

When the presence of a fault in the terminal is obvious (dead terminal, bad display, etc) refer to the troubleshooting procedure, paragraph 2.4. Otherwise confirm that the fault is in the terminal, and not in the line interface or computer. If more than one terminal is available at the site, this may be accomplished by interchanging terminals. If the fault involves only full duplex operation, or received data only, and only one terminal is available, proceed as follows:

NOTE

For the model 1500 when operating at rates of 2400 baud or higher, some fill characters from the computer may be required to permit proper response to remote commands without loss of data (refer to the Reference

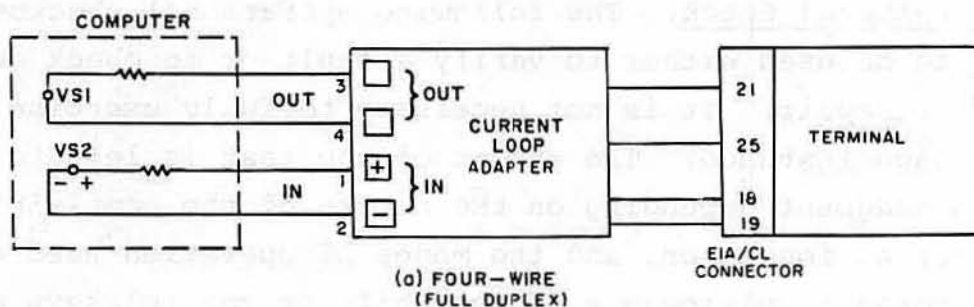
Manual). Failures of this nature cannot be duplicated with a single terminal; only substitution will confirm or eliminate the terminal as the cause of the failure. This may be done by substituting a spare keyboard/logic assembly (after checking voltages in accordance with paragraph 2.4.2) if a second terminal is not available.

- a. Connect the current loop adapter for half duplex operation as shown in figure 2-1(b) or connect a jumper adapter as shown in figure 2-1(c). This routes the terminal output data back to the terminal as input data.
- b. Set the power switch on and check that the red POWER ON indicator is lit.
- c. Set the HALF DUP/FULL switch to FULL.
- d. Set the EIA/CUR LOOP switches to CUR LOOP, if a current loop adapter is used, or to EIA if a jumper adapter is used.
- e. Perform those portions of the checkout procedure, paragraph 2.2.2, necessary to confirm or eliminate the terminal as the cause of the fault.

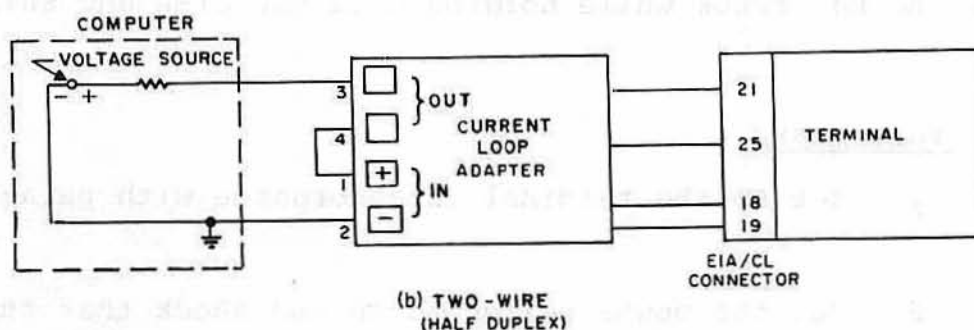
2.2.2 Checkout Procedure

Perform the following checkout procedure to verify proper operation of the terminal following repair. Portions of the procedure may be used as necessary to confirm the existence of a fault. If the installation does not provide for full duplex operation, omit that part of the procedure. If the installation uses only full duplex, omit the half duplex part.

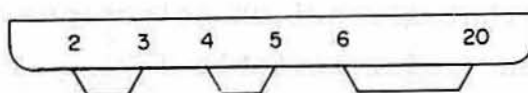
2.2.2.1 Setup. Several options are available depending on the type of installation and the nature of the problem. As a checkout of the terminal, it is preferable that the test be performed with the terminal installed in the normal manner for the site. In order to check input/output operation fully in half duplex operation, it will be necessary to store the data generated by the terminal and then retransmit it to the terminal. In order to isolate the terminal



a) Four-Wire (Full Duplex)



b) Two-Wire (Half Duplex)



DB25P CONNECTOR
EIA FEMALE HOUSING
WITH MALE PINS.

c) Jumper Adapter

Figure 2-1. Current Loop Interface and Full Duplex Jumper Adapter from the interface and/or to minimize interference with system operation during troubleshooting, the following setups may be used.

a. Full Duplex. Connect the current loop adapter as shown in b of figure 2-1, and select current loop operation, or connect a jumper adapter (c of figure 2-1) to the EIA/CL connector, and select EIA operation.

b. Half Duplex. The terminal operates with no external data connections. This is satisfactory for checking keyboard operation, response, and display, but cannot verify proper transmitted data or proper response to received data. The terminal may also be connected back-to-back with another terminal if an adapter, as shown in figure 4-3, is available. Use the second terminal to verify that proper data is transmitted, and to generate inputs to the terminal under test.

2.2.2.2 Operational Check. The following operational checkout procedures are to be used either to verify a fault or to check out a terminal after repair. It is not necessary to fully exercise every function in each instance. The extent of the test is left to the technician's judgment depending on the nature of the complaint, the type of repair action taken, and the modes of operation used at the site. Keystrokes involving use of the shift or control keys are preceded by a superscript c, s, or both. Thus, ^{CS}0 indicates that the 0 key is to be struck while holding both the CTRL and SHIFT keys down.

a. Preliminary

1. Set up the terminal in accordance with paragraph 2.2.2.1.

2. Set the power switch to on and check that the red POWER ON indicator is lit. Check that the screen is clear with the cursor at the home position within 1 minute.

3. Verify that all switch selections conform with the norm for the installation (refer to table 1-2).

4. Adjust CONTRAST control to obtain suitable display.

NOTE

For 1510/1520 models, substitute ESC for ^S~ if that option is selected.

b. Half Duplex

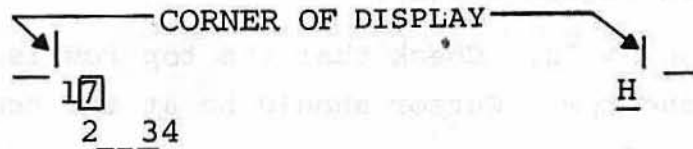
1. Set the HALF DUP/FULL switch to HALF DUP.

2. Type the following sequence as a quick check of terminal operation (use the alphanumeric cluster keys for some numbers, and the numeric cluster for some numbers):

1 ^S~ ^Ck 2 ^S~ ^{CS}0 space space 3 ^S~ ^Cy 4 ^S~ ^{CS}0 ^S~ ^CQ ^S0
^Cspace ^SH ^S~ ^CQ ^Cspace w ^SH ^S~ ^Cy ^SLINE FEED 5 (set ALL CAPS)
a 6 (release ALL CAPS) b p HOME ^SBACK SPACE 7 BACK SPACE

The display should appear as in figure 2-2(a). Underlined areas should be in high intensity. The cursor and the character "7" should interchange three times per second.

3. Change the STD VIDEO/REV switch setting and check that the video is reversed.



(a)



(b)

7704102

Figure 2-2. Displays for Checkout Procedure

4. Type $\overset{C}{\text{CLEAR}}$. Check that the characters 7 and H are cleared from the top line and the cursor does not move.

NOTE

If the preceding data is recorded and played back to the terminal, the display should appear as shown in figure 2-2(b).

5. Type $\overset{S}{\sim} \overset{C}{\text{s}}$. Check that the top row is deleted and all others move up one row. Cursor should be at the home position.

6. Type $\overset{S}{\text{LINE FEED}}$. The display should not change.

7. Type $\overset{S}{\text{CLEAR}}$. Check that the intensified spaces and "H" are cleared to foreground spaces. The cursor should be at the home position.

8. Type $\overset{S}{\sim} \overset{C}{\text{z Q W E R T Y BACK SPACE}}$. The characters "q w e r t y" should appear on the top row with the cursor superimposed on the "y". All other characters should drop one row.

9. Type $\overset{S}{\sim} \overset{C}{\text{x}}$. The "y" and all characters after it should be cleared to spaces. The cursor should not move.

10. Hold the RETURN key (if the AUTO LF mode is selected) or the LINE FEED key (if the CR mode is selected) down to move the cursor to the bottom row of the screen.

11. Press the RETURN or LINE FEED key one more time, followed by any character. The character typed should appear on the bottom row and the top row should be cleared.

12. Press the CLEAR key. The screen should be cleared to foreground spaces and the cursor should be at the home position.

13. Type $\overset{S}{\sim} \overset{CS}{\text{O a s}} \overset{S}{\sim} \overset{C}{\text{u d d}}$. Only the intensified characters "a" and "s" should appear on the screen (the keyboard should be locked out).

14. Press the BREAK key. The display should not change and the keyboard should remain locked out.

15. Press the RESET key. The screen should be blanked briefly and then the original display should reappear. The key-

board should be unlocked and typed characters should appear at low intensity.

16. 16. Type C_g . The audible alarm should sound.

c. Full Duplex

1. Set the HALF DUP/FULL switch to FULL.

NOTE

The results of the following procedures depend upon all characters generated by the terminal being echoed back to the input. This may be accomplished with the setup shown in figure 2-1(b) or with a jumper connector as shown in figure 2-1(c). If the terminal is checked out on line in a system which does not always echo back the generated characters, different responses will be obtained.

2. Perform steps 2 and 3 of the half duplex procedure given in paragraph b above.

3. Type TAB twice. The cursor should move over the first "H" and then over the first intensified space.

4. Type $S_{\sim} C_L$ BACK SPACE C_{CLEAR} . Check that the "7" and "H" are deleted from the top line and the cursor is in the position formerly occupied by the "7".

5. Perform steps 5 through 8 of the half duplex procedure given in paragraph b above.

6. Type C_x . The "Y" and all characters after it should be cleared to spaces. The cursor should not move.

7. Perform steps 10 through 16 of the half duplex procedure given in paragraph b above.

CURSOR
MOVED RIGHT
ONCE
THEN DOWN
ONE ROW

NO CHANGE

d. Format Mode (1510/1520 only)

1. Make the following switch settings:
 WRAPAROUND: YES ESC/~: Norm for installation
 FORMAT: Off EOM A&B: Norm for installation
2. Type a half row of characters.
3. Type $S_{\sim}S_{\#}$ and check that the FORMAT LED comes on.
4. Depress and hold any character. Check that characters appear in foreground intensity and the display wraps around at the right hand margine.
5. Press CLEAR. The display should not change.

NOTE

If a jumper adapter, as in figure 2-1 c, is being used, disconnect it.

6. Press SEND. A transmit symbol (■) should appear at the present cursor position and the cursor should advance to the start of the next line.
7. Press ↑. The cursor should move up one line.
8. Press C CLEAR. The line the cursor is on should be cleared.
9. Press S CLEAR. All foreground characters should be cleared.
10. Press HOME and CLEAR. The cursor should home and the screen should be cleared.
11. Press RESET. The FORMAT LED should go out.

e. Printer Buffer (1520 only)

1. Put the printer on line (by switch or by typing $S_{\sim}/$).
2. Enter some random characters on the top line. Check that the characters are printed.

3. Type $S \sim S \#$. The FORMAT LED should come on.
4. Enter some random characters followed by RETURN.
5. Hold any character key down to fill the screen. The cursor should stop at the end of the bottom row and the alarm should sound.
6. Move the cursor to the top line and to the right of the carriage return entered in step 4. Enter a few additional characters.
7. Move the cursor to the last character position on the bottom row and press S PRINT. The alarm should sound.
8. Move the cursor left one character and type S PRINT. A print symbol (■) should appear at the cursor position, the cursor should move to the start of the bottom row, and all data preceding ■ should be printed except the characters to the right of the carriage return on the top line. Characters typed after the FORMAT LED stops blinking should appear on screen even if printing is not completed.

NOTE

If the printer automatically does a carriage return/line feed at the end of an 80 character row, the resulting print-out should be double spaced from the second row down for step 8, but single spaced for step 9.

9. Type SEND. All foreground data should be printed except the bottom row and data to the right of the carriage return on the top row.

2.3 ACCESS

WARNING

Dangerous voltages (15 K vdc and 115 vac) are present in the terminal, and high voltage may be retained in the monitor circuits after power is removed. Exercise caution when working within the unit.

2.3.1 To gain access to the internal components, reach under the unit and release two captive screws at the front corners, and two captive screws at the sides approximately in line with the crt face. Then release two captive screws at the upper part of the back of the unit. The cover, including the monitor may be lifted off the base assembly. The wiring allows sufficient slack to lay the cover upside down alongside the base, facilitating access to the monitor components.

CAUTION

The keyboard/logic assembly is secured only by one screw near the input/output connectors. Do not turn the base assembly over once the screws securing the cover are released.

2.3.2 The power transformer, printer buffer and 5-volt regulator are located under the keyboard/logic assembly. Disconnect all connectors to logic board, remove the screw securing the logic board to the base, and lift the board up at the rear to gain access to these units.

2.4 TROUBLESHOOTING

2.4.1 Scope

This section provides troubleshooting data to aid in isolating a fault to one of seven removable subassemblies. The relationship of the sub-assemblies is shown in figure 2-3. Since all keyboard, logic, and input/output functions are performed by the keyboard/logic assembly, no further isolation is required in these areas. Use the checkout procedures of paragraph 2.2.2 as necessary to confirm or eliminate the terminal as the cause of a fault. Table 2-1 defines

Table 2-1. Terminal Operation - Functions
Part One - Model 1500

FUNCTION	KEY STROKE (S)	HALF DUPLEX			FULL DUPLEX	
		CHAR(S) SENT	DO FUNCTION WHEN KEYED	DO FUNCTION WHEN RECEIVED	CHAR(S) SENT	DO FUNCTION WHEN RECEIVED
Direct Cursor Address ¹	~ c _Q	~ DC1	No	Yes	~ DC1	Yes
Read Cursor Address	~ c _E	~ ENQ	No	Yes ²	~ ENQ	Yes ²
Home Cursor	HOME	No	Yes	If preceded by ~	~ DC2	Yes
Up Cursor	^S LINE FEED	No	Yes	If preceded by ~	~ FF	Yes
Down Cursor	~ c _K	~ VT	No	Yes	~ VT	Yes
Left Cursor	BACK SPACE	No	Yes	Yes	BS	Yes
Right Cursor	^S BACK SPACE	No	Yes	Yes	DLE	Yes
Foreground Tab	TAB	HT	Yes	Yes	HT	Yes
Clear Screen	CLEAR	No	Yes	If preceded by ~	~ FS	Yes
Set Background	~ c _Y	~ EM	Yes	Yes	~ EM	Yes
Set Foreground	~ cs _O	~ US	Yes	Yes	~ US	Yes
Audible Alarm	c _G	BEL	Yes	Yes	BEL	Yes
Keyboard Lock	~ c _U	~ NAK	Yes	Yes	~ NAK	Yes
Keyboard Unlock	~ c _F	~ ACK		Yes	~ ACK	Yes
Delete Line	~ c _S	~ DC3	Yes	Yes	~ DC3	Yes
Insert Line	~ c _Z	~ SUB	Yes	Yes	~ SUB	Yes
Clear to end-of-line	c _{CLEAR}	No	Yes	If preceded by ~	~ SI	Yes
Clear to end-of-screen	cs _{CLEAR}	No	Yes	If preceded by ~	~ CAN	Yes
Clear Foreground	^S CLEAR	No	Yes	If preceded by ~	~ GS	Yes
Clear to end-of screen (back-ground)	~ c _W	~ ETB	Yes	If preceded by ~	ETB	Yes

Table 2-1. Terminal Operation - Functions
Part Two - Models 1510 and 1520

Function	Key Stroke(s)	Half Duplex			Full Duplex ¹ Char(s) Sent	Format ² When Keyed
		Char(s) Sent	Do When Keyed	Do When Received		
Direct Cursor Address	~ ^C Q	~ DC1	No	Yes	~ DC1	Store ~ DC1
Read Cursor Address	~ ^C E	~ ENQ	No	Yes	~ ENQ	Store ~ ENQ
Home Cursor	HOME	No	Yes	Yes	~ DC2	Do
Up Cursor	↑ or ^S LINE FEED	No	Yes	If prec. by ~	~ FF	Do
Down Cursor	↓	No	Yes	If prec. by ~	~ VT	Do
Left Cursor a)	←	No	Yes	Yes	BS	Do
b)	BACK SPACE	BS	Yes	Yes	BS	Store BS
Right Cursor a)	→	No	Yes	Yes	DLE	Do
b)	^S BACK SPACE	DLE	Yes	Yes	DLE	Store DLE
Foreground Tab	TAB	HT	Yes	Yes	HT	*Do
Clear Screen	CLEAR	No	Yes	If prec. by ~	~ FS	*Do if home
Clear-to-end-of-line	^C CLEAR	No	Yes	If prec. by ~	~ SI	*Do
Clear-to-end-of-screen	^{CS} CLEAR	No	Yes	If prec. by ~	~ CAN	*Do
Clear foreground	^S CLEAR	No	Yes	If prec. by ~	~ GS	*Do
Clear-to-end-of screen (bkgn)	~ ^C W	~ ETB	Yes	If prec. by ~	~ ETB	*Store ~ ETB
Set Background	~ ^C Y	~ EM	Yes	Yes	~ EM	Store ~ EM
Set foreground	~ ^{CS} O	~ US	Yes	Yes	~ US	Store ~ US
Audible alarm	^C G	BEL	Yes	Yes	BEL	Do
Keyboard Lock	~ ^C U	~ NAK	Yes	Yes	~ NAK	Store ~ NAK
Keyboard unlock	~ ^C F	~ ACK		Yes	~ ACK	
Delete line	^S D/L	~ DC3	Yes	Yes	~ DC3	*Do
Insert line	^S I/L	~ SUB	Yes	Yes	~ SUB	*Do
Back tab	^S TAB	DC4	Yes	Yes	DC4	*Do
Send status	~ hyphen	Status Word	Yes	Yes	~ -	Store ~ -
Print (1520 only)	^S PRINT	No	Yes	Yes (~ ^{CS} N)	No	*Do
Function	FUNCTION A/N Char	ESC A/N char EOM			ESC A/N Char EOM	*Send ESC A/N Char EOM

Notes for Tables 2-1 Part One

1. Function must be followed by X and Y coordinates.
2. Cursor X and Y coordinates will be sent, followed by CR.
3. The following ASCII codes will be sent when the indicated key(s) are struck. Nothing will be displayed when sent, and no action will be taken if received.

Code: NUL SOH STX ETX EOT SO RS DC4 SYN ESC DEL

Key: c_p c_A c_B c_C c_D c_N cs_N s_{TAB} c_V ESC DEL

4. If the AUTO LF/CR switch is set to AUTO LF, depressing the RETURN switch causes the CR and LF codes to be sent, in either half or full duplex, and both operations are executed. Both operations will be performed if a CR is received. The LINE FEED key will cause a LF to be sent, but nothing will be displayed and no operation will be performed when sent or if received.
If CR is selected, a CR will be sent when the RETURN key is depressed. The cursor will move to the beginning of the present line when the character is sent or received. A LF will be sent the LINE FEED key is depressed. The cursor will move down one row when the character is sent or received.
5. All characters/functions will be repeated at a rate of 15 per second if the key(s) is depressed longer than 3/4 second (typamatic operation) except: HOME, all CLEAR functions, and the BREAK key.
6. The BREAK key causes a 250 ms interruption in output. Received data and the auxiliary output are not affected.
7. Cursor Up/Down will not be performed if the cursor is on the top/bottom row. Cursor right/left commands will cause cursor wraparound if the cursor is at the edge of the screen.

Notes for Table 2-1 Part Two

1. All functions are performed when command is received (or echoed) in full duplex.
2. All functions are performed when command is received in format mode (including clear screen regardless of cursor position). Functions noted with an * will not be performed if received or keyed during a transmission.
3. The following keystrokes will cause an alarm in half or full duplex: SEND, c_{SEND}, cs_{SEND}, LOCAL
4. Substitute ESC for ~ in all cases if that option is selected by switch.

the normal terminal outputs, displays, and response to inputs. Removal and replacement procedures are given in paragraph 2.6.

2.4.2 Procedure

Tables 2-2 and 2-3 provide information to assist in isolating faults to replaceable subassemblies. Check the voltage inputs before replacing the keyboard/logic assembly or the monitor electronics to ensure that a fault in the power circuits is not the cause of a problem. No-load voltages are given to enable isolation of an undervoltage condition between the source and a overload condition in the load. Disconnect the load from the source to check. Input resistances are given to aid in troubleshooting when power cannot safely be applied. Check with power off and the input disconnected. When a fault is isolated to the monitor, and it is not obvious whether the fault is in the electronics chassis or the crt yoke assembly, further isolation may be done by substitution.

2.5 ADJUSTMENTS

2.5.1 Five-Volt Regulator.

Adjust the 5-volt regulator (refer to figure 2-3) as follows:

NOTE

Do not change the setting of R18 or R19 at the site. Additional test equipment is required to make these adjustments.

- a. With power off, disconnect the lead from terminal 4 of the regulator assembly.
- b. Connect a voltmeter between terminal 4 and chassis ground.
- c. Turn power on.
- d. Adjust +5 V potentiometer R8 for a 5.20 vdc indication.
- e. Turn power off and reconnect the lead to terminal 4.

Table 2-2. Voltage and Resistance Data

TP	Test Point	Normal	No Load Voltage	Impedance
A	T1 terminals 1 & 2	115 ±12 vac	Same	4 Ω max.
B ₁	5 V rgltr CR3-1/E2	10 vac	11 vac	5000 Ω if CR3-1+; 3000 Ω initially, >10K after capacitor charges if E2+
B ₂	CR3-3/E2	10 vac	11 vac	3000 Ω initially, >10K after capacitor charges if CR3-3+; 5000 Ω if E2+
+5 V	Test connector pins 49 & 32	5.2 ±0.25 vdc	5.2 vdc at 5 V rgltr E4 & E5	6 Ω (P102-2 +) 14 Ω (P102-4 +)
C ₁	BR1 (∞), Test connector pin 32	14 vac	15 vac at J102-1, -6	5000 Ω (P102-1 +) 5000 Ω (P102-6 +)
C ₂		14 vac	15 vac at J102-3, -6	5000 Ω (P102-3 +) 5000 Ω (P102-6 +)
D	U3	75 vac	80 vac at J8-2, -3 gray, white	>15K (P8-2 +) >15K (P8-3 +)
PRINTER BUFFER BOARD				
E	J2-18/J2-73	-12 vdc		
F	J2-16/J2-73	+12 vdc		
G	J2-19/J2-73	+5.2 ±0.25 vdc		
H	J2-73	GND		
NOTE				
Impedance values will vary depending on the voltages used by the meter. They are provided primarily as an aid in isolating catastrophic failures.				

Table 2-3. Troubleshooting Chart

TROUBLE	ISOLATION PROCEDURE
Circuit Breaker Tips	With no power connected, check input impedance at test points B through D (figure 2-3 and Table 2-3). If no fault is found, replace T1.
Dead Terminal	Check voltages at test points A through D and +5 vdc (figure 2-3 and table 2-3).
No Display	<ol style="list-style-type: none"> 1. Check F1 on monitor circuit board. 2. Check voltage at test point D (figure 2-3 and table 2-3). 3. Type CG. The alarm should sound for 1/3 second. If missing or excessively long or short, keyboard/logic assembly is faulty. 4. Adjust brightness control R26. If no raster appears, monitor is faulty. 5. If another terminal is available, connect cover and monitor assembly to faulty terminal (J101 and P8 of monitor to P101 and J8 of keyboard/logic assembly) to isolate fault between monitor and keyboard/logic assembly.
Distorted Display	Align monitor in accordance with paragraph 2.5.2.

f. Turn power on and check for 5.2 ± 0.25 volts across capacitor C68.

2.5.2 Monitor Adjustments

Adjust the monitor as follows:

a. Preliminary

1. Turn power on.
2. Set the STD VIDEO/REV switch to STD VIDEO, and the HALF DUP/FULL switch to HALF DUP.
3. Adjust BRIGHT control R26 until the raster is just extinguished. (All adjustments are located along the back edge of the monitor circuit board.) This adjustment should be made within 1 minute of turn on.
4. Type several full rows of characters spaced from top to bottom of the screen.
5. Adjust the CONTRAST control for suitable contrast.

b. Vertical Adjustments

1. Adjust VERT SIZE control R36 for desired height.
2. Adjust VERT LIN control R39 for best vertical linearity. Readjust R36 as required.

c. Horizontal Adjustments

1. Adjust BRIGHT control R26 until the edge of the raster can be seen.
2. Adjust HORIZ HOLD control R5 clockwise until sync is lost.
3. Adjust R5 slowly counterclockwise until sync is just restored. Note the position of the adjustment.
4. Adjust R5 counterclockwise until sync is lost again.
5. Adjust R5 clockwise until sync is just restored.
6. Set R5 midway between the points noted in steps 3 and 5.
7. Measure the gap between the 80th character on the top line and the right edge of the raster. If the gap is less than $1/16$ inch, proceed as follows:

(a) Adjust HORIZ HOLD control slowly clockwise and watch the 80th character for a 1/8 inch jump to the left.

(b) If the horizontal hold cannot be adjusted so the gap is 1/16 inch or greater without losing sync, replace the monitor electronics.

8. Readjust BRIGHT control R26 until the raster is just extinguished.

9. Turn power off and on. The monitor should synchronize within 2 seconds. Readjust R26 if necessary.

NOTE

R57 also adjusts the B+ supply for monitor electronics. If any subsequent change is made, repeat other adjustments.

d. Centering. If the display is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke.

NOTE

(1) The ring magnets should not be used to offset the raster from the nominal center position because it will degrade the resolution of the display.

(2) The HORIZ HOLD control should not be used to adjust video centering within the raster. The control is to be left in the center of the pull-in points in order to maintain horizontal sync.

e. Focus Adjustment

1. Adjust dynamic focus control L3 (located near FOCUS potentiometer R22) for 150 volts rms at the junction of C18 and L3.

2. Adjust static FOCUS potentiometer for best overall focus at normal contrast level.

2.6 REMOVAL AND REPLACEMENT

2.6.1 Monitor Electronics Chassis

WARNING

Hazardous voltage may be present in the CRT anode circuit. The anode lead must be discharged before working on the CRT or monitor circuit board.

2.6.1.1 To remove the electronics chassis, refer to figure 2-5 and proceed as follows:

- a. Disconnect the anode lead from the side of the crt (pull out). Use a screwdriver to ground the anode lead to the chassis.
- b. Disconnect P1 from the back edge of the circuit board, and P3 from the front edge of the board.
- c. Separate flying lead connectors P8 and J8.
- d. Disconnect P6 from the crt base socket.
- e. Turn the cover and monitor upside down.
- f. Remove and retain two screws and lock washers from each side of the chassis.

CAUTION

There are connections to heat sink mounted components between the sides of the cover and the chassis. Use caution when removing the chassis.

- g. Carefully lift the chassis straight up.

2.6.1.2 To replace an electronics chassis, slide it carefully into the cover and secure the fasteners and connections shown in figure 2-4, being sure that the ground lug is secured at one corner of the chassis.

2.6.2 CRT/Yoke Assembly and Video Filter.

2.6.2.1 To remove the crt/yoke assembly, refer to figure 2-5 and proceed as follows:

- a. Disconnect the anode connector from the side of the crt (pull out). Use a screwdriver to ground the anode lead to the chassis.
- b. Disconnect P6 from the crt base connector.
- c. Disconnect P3 from the inside edge of the electronics board.

WARNING

Use caution when handling the cathode-ray tube to avoid risk of implosion. The internal phosphor coating is toxic. If the tube breaks and skin or eyes are exposed to phosphor, rinse with cold water and consult a physician.

- d. Remove and retain two screws and washers securing each of two brackets to the cover.
- e. Carefully remove the crt, along with the video filter, yoke and brackets, from the cover.
- f. Remove the ground spring from the brackets.
- g. Remove and retain the four screws and nuts securing the CRT to the brackets.

2.6.2.2 To replace a crt yoke assembly, proceed as follows:

- a. Secure the two brackets to the crt using the four screws and nuts retained in step g above.
- b. Attach the ground spring to the two holes in the brackets.
- c. Place the video filter on the crt face and carefully align the assembly with the mounting holes in the cover.
- d. Secure the fasteners and connections shown in figure 2-5, being sure the ground lug is secured to one bracket.

2.7 CLEANING VIDEO FILTER

2.7.1 The video filter may be cleaned with a soft cloth and household glass cleaner.

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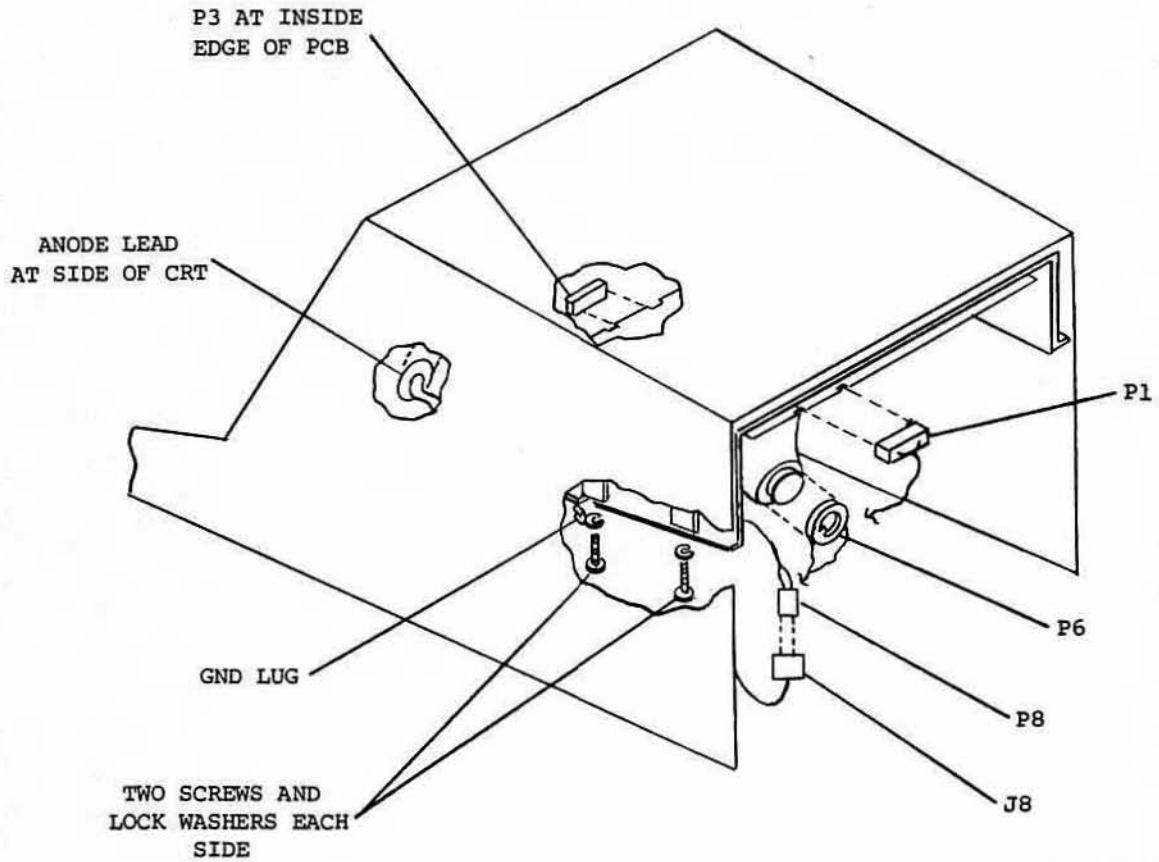


Figure 2-4. Monitor Electronics Chassis

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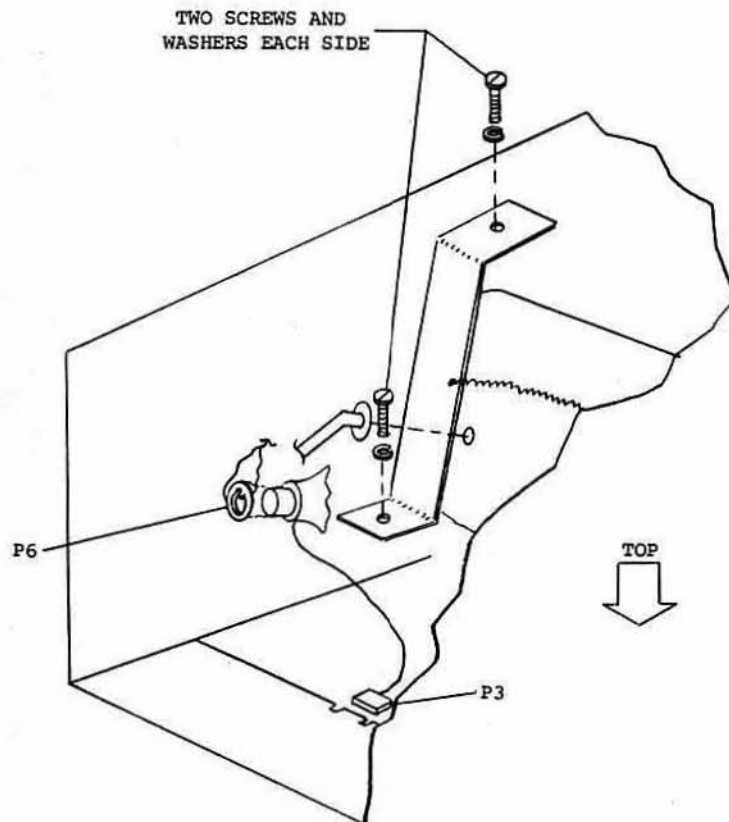


Figure 2-5. CRT/Yoke Assembly

2-21/(2-22 blank)

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REPAIR SHOP MAINTENANCE

3.1 INTRODUCTION

3.1.1 Scope

This section provides checkout, troubleshooting and alignment procedures for the monitor electronics and for the 5-volt regulator assembly. Refer to Appendix A for recommended spare parts, and to Appendix B for component location and schematic diagrams.

3.1.2 Tools and Test Equipment

The following tools and test equipment are required for shop maintenance:

Oscilloscope, Tektronix 465 or equivalent

Hot mock-up test bed

Ammeter, 0 to 15 A, dc

Variable Transformer, 0 to 140 vac, 5 A, 60 Hz

Regulator Test Jig

Standard Serviceman's Kit including:

- Hand Tools
- Alignment Tools
- Volt-Ohmmeter, digital
- Spare Parts Allocation (Refer to Appendix A)

The hot mock-up test bed is a model 1500 terminal with a transparent size/centering overlay as shown in figure 3-1. The regulator test jig is shown in figure 3-3.

3.2 CHECKOUT

3.2.1 Monitor Electronics Chassis

The following checkout procedure may be used to determine the condition of an electronics chassis returned for repair, or to verify proper operation following repair and adjustment. The procedures include adjustments required to make the unit ready for use.

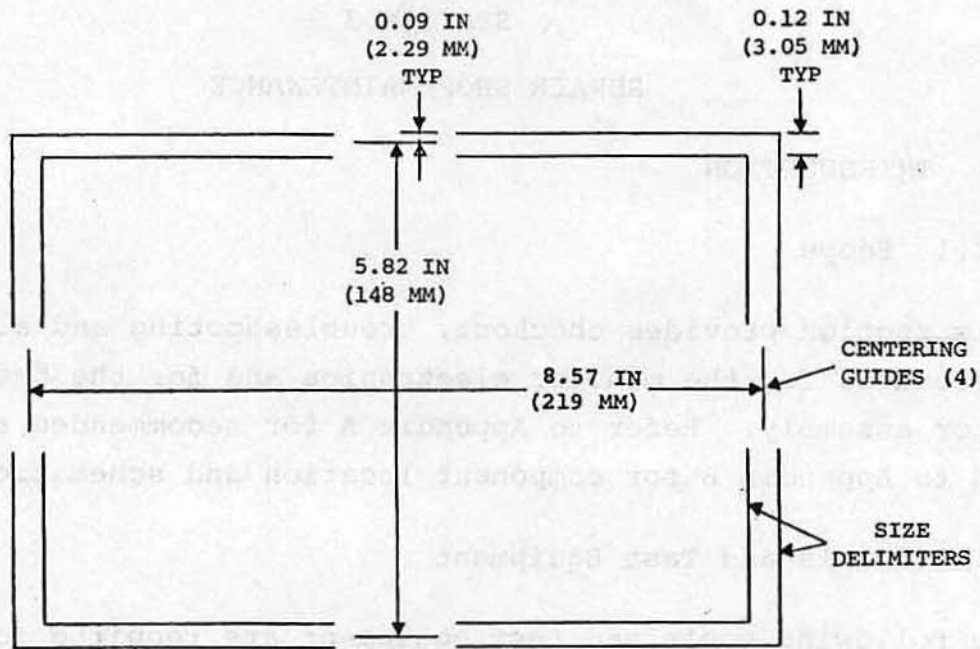


ILLUSTRATION NOT TO SCALE

Figure 3-1. Size/Centering Overlay

3.2.1.1 Setup. Connect the chassis to the hot mock-up test bed and perform the following preliminary steps:

1. Set WIDTH potentiometer R57 fully clockwise.
2. Set L3 (dynamic focus coil) for maximum inductance (slug completely within coil form).
3. Set the FULL DUP/HALF switch to HALF, and the NORM VID/REV switch to NORM VID.
4. Set the power switch to on.

NOTE: The first nine steps of the checkout procedure should be performed within 3 minutes of turn on.

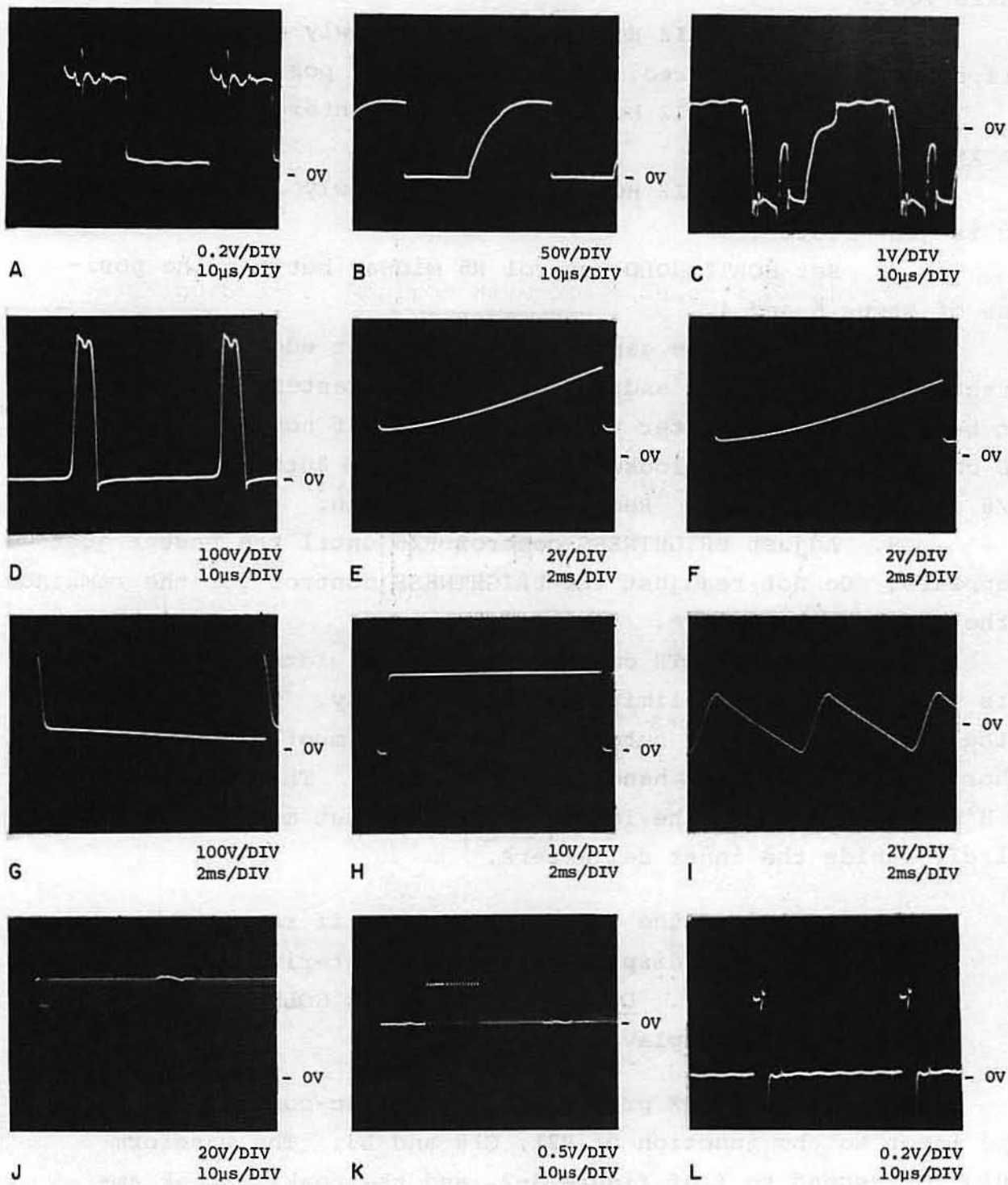
3.2.1.2 Checkout Procedure. Perform the entire procedure to check out a chassis after repair. For troubleshooting, omit those alignment procedures unrelated to the fault.

1. Enter four full rows of H characters on the first, ninth, seventeenth and twenty fourth (bottom) rows.

2. Adjust BRIGHTNESS control R26 until both the video and raster are visible.
3. Adjust HORIZ HOLD control R5 slowly clockwise until sync is lost.
4. Adjust HORIZ HOLD control R5 slowly counterclockwise until sync is just restored. Note the control position.
5. Adjust HORIZ HOLD control R5 counterclockwise until sync is lost.
6. Adjust HORIZ HOLD control R5 slowly clockwise until sync is just restored.
7. Set HORIZ HOLD control R5 midway between the positions of steps 6 and 4.
8. Measure the gap between the right edge of the 80th character on the top row and the edge of the raster. The gap must be equal to or greater than 1/16 inch. If not, adjust HORIZ HOLD control R5 slowly clockwise and watch the 80th character for a 1/8 inch jump to left. Recheck the gap width.
9. Adjust BRIGHTNESS control R26 until the raster just disappears. Do not readjust the BRIGHTNESS control for the remainder of the checkout procedure.
10. Adjust WIDTH control R57 so the width of the display falls within the size delimiters on the overlay. The outside edge of the H's may touch the outer delimiters but must not fall outside either the right or left hand outer delimiter. The outer edge of the H's may just touch the inside delimiters but must not fall entirely inside the inner delimiters.

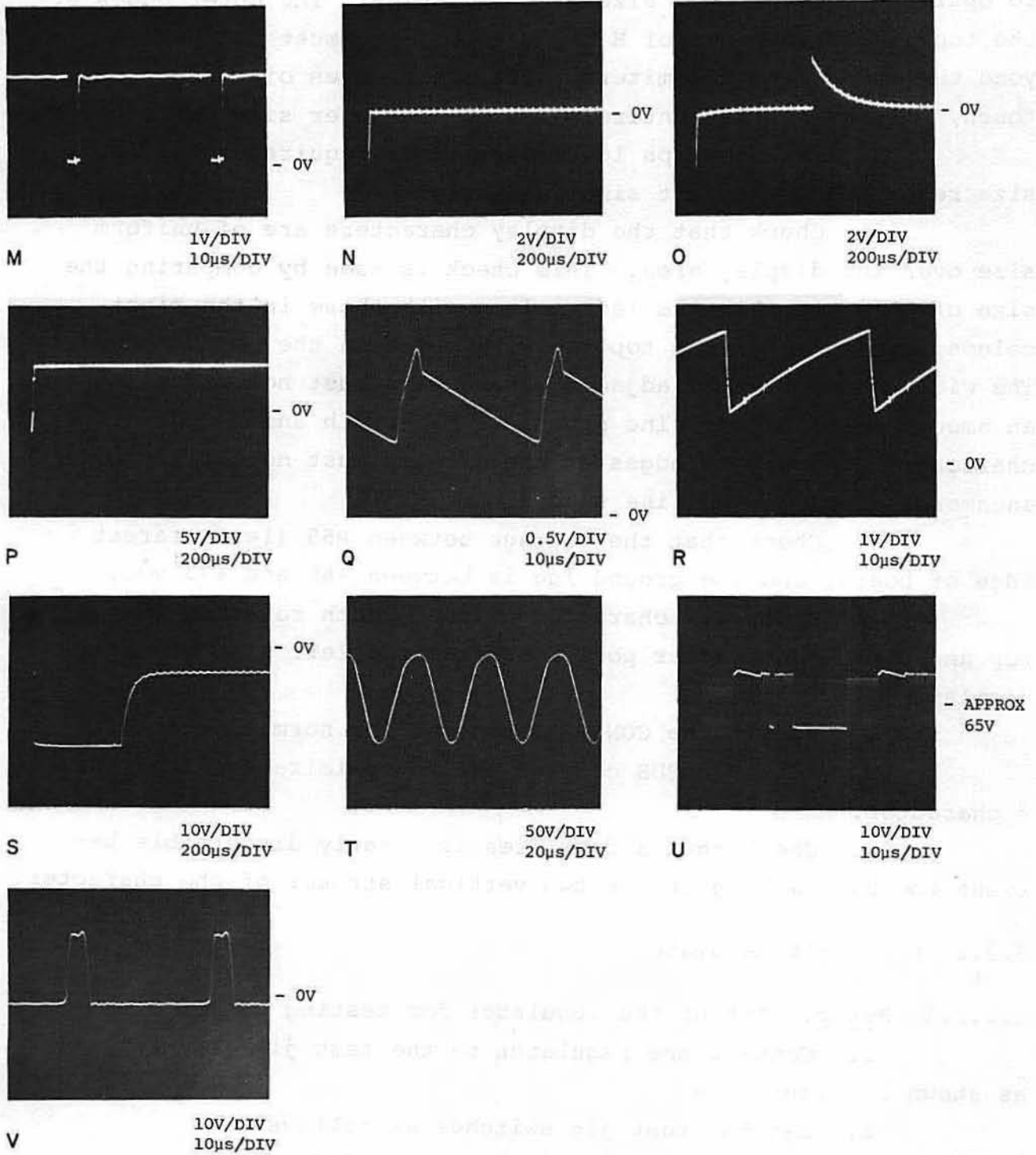
NOTE: Adjust the yolk ring magnets if required to center the display within the centering guides on the overlay. Do not adjust HORIZ HOLD control to improve display centering.

11. Using a 10X probe, connect the ac-coupled oscilloscope input to the junction of R21, C18 and L3. The waveform should correspond to T of figure 3-2, and the peak-to-peak amplitude must be between 160 and 240 volts.



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Figure 3-2. Monitor Waveforms (Sheet 1 of 2)



7704105

Figure 3-2. Monitor Waveforms (Sheet 2 of 2)

12. Adjust FOCUS control R22 for best overall focus.

13. Adjust VERT SIZE control R36 and VERT LIN control R39 to optimize the vertical size of the display. The outer edges of the top and bottom rows of H's may touch, but must not extend beyond the outer size delimiters. The outer edges of the H's may touch, but may not lie entirely inside the inner size delimiters.

14. Repeat steps 10 through 13 as required until all size requirements are met simultaneously.

15. Check that the display characters are of uniform size over the display area. This check is made by comparing the size of characters in the left column with those in the right column, and those on the top row with those on the bottom row. The width and height of adjacent characters must not differ by an amount equal to one line spacing. The width and height of characters at opposite edges of the display must not differ by an amount equal to two line spaces.

16. Check that the voltage between R55 (lead nearest edge of board) and the ground lug is between +65 and +75 vdc.

17. Enter a # character in the eighth row from the top and sixteen character positions from the left side of the display.

18. Adjust the CONTRAST control for normal contrast.

19. Adjust FOCUS control R22 to optimize focus of the # character.

20. Check that a dark area is clearly discernible between the dots making up the two vertical strokes of the character.

3.2.2 Five-Volt Regulator

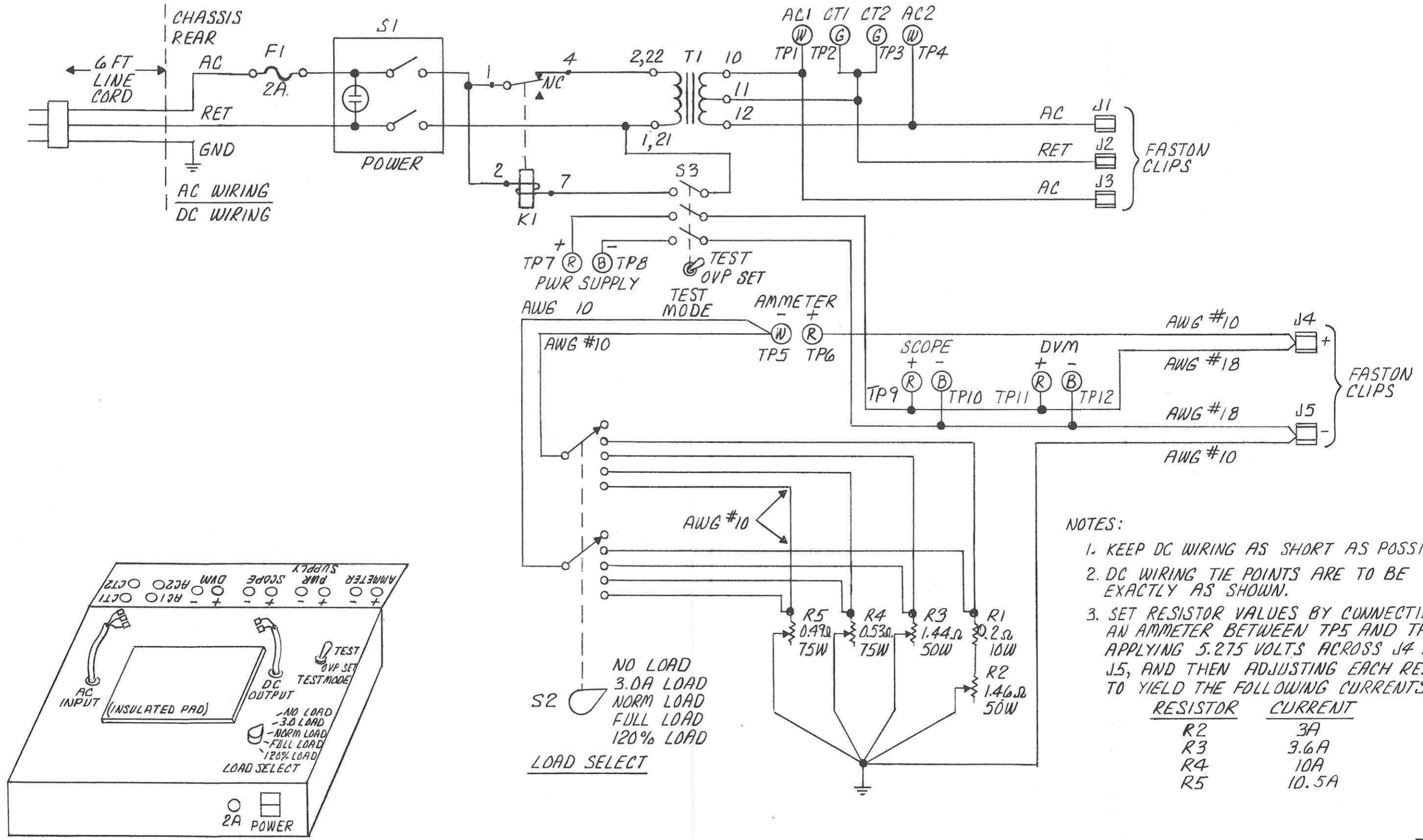
3.2.2.1 Setup. Set up the regulator for testing as follows:

1. Connect the regulator to the test jig (figure 3-3) as shown in figure 3-4.

2. Set the test jig switches as follows:

LOAD SELECT switch	- NO LOAD
TEST MODE switch	- TEST
POWER switch	- OFF

3. Set the variable transformers for a nominal 120 vac.



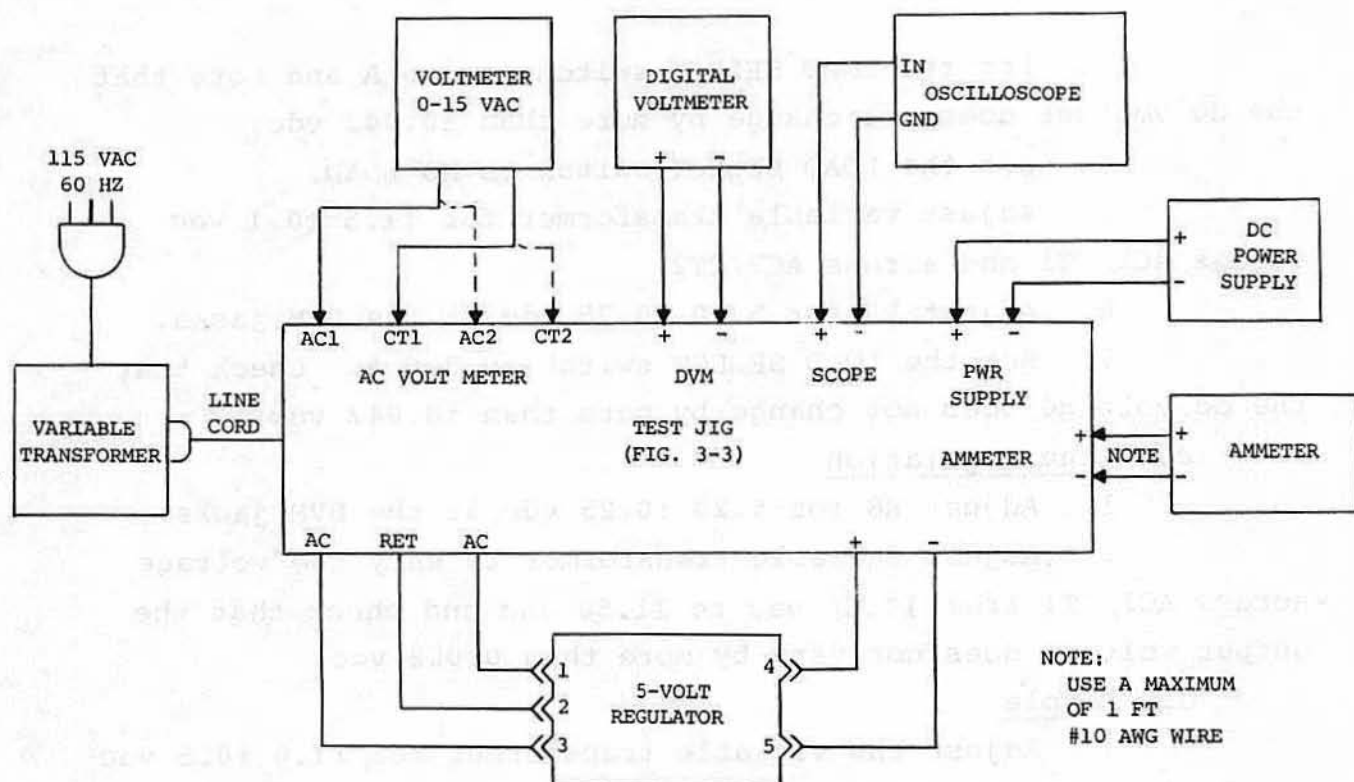
- NOTES:
1. KEEP DC WIRING AS SHORT AS POSSIBLE.
 2. DC WIRING TIE POINTS ARE TO BE EXACTLY AS SHOWN.
 3. SET RESISTOR VALUES BY CONNECTING AN AMMETER BETWEEN TP5 AND TP6, APPLYING 5.275 VOLTS ACROSS J4 AND J5, AND THEN ADJUSTING EACH RESISTOR TO YIELD THE FOLLOWING CURRENTS:
- | RESISTOR | CURRENT |
|----------|---------|
| R2 | 3A |
| R3 | 3.6A |
| R4 | 10A |
| R5 | 10.5A |

Figure 3-3. Five-Volt Regulator Test Jig (Sheet 1 of 2)

ITEM	QTY	IDENT.	DESCRIPTION	MANUFACTURER	PART NUMBER
1	2	R5, R4	Slide-Wire Resistor 0 to 1 ohm, 150W	Ohmite	1156A (150W)
2	2	R3, R2	Slide-Wire Resistor 0 to 2 ohm, 50W	Allied	8801203 (0-2 ohm)
3	1	R1	Fixed Resistor 0.2 ohm, 10W	Dale	RS-10 0.2 ohm, 10W
4	-	-	5 Way Binding Posts:		
a	3	TP8, 10, 12	-Black	H. H. Smith	257-0
b	4	TP6, 7 9, 11	-Red	H. H. Smith	257-2
c	3	TP1, 4	-White	H. H. Smith	257-9
d	2	TP2, 3	-Green	H. H. Smith	257-5
5	1	S1	Rocker Switch, AC		
6	1	S2	Non-Shorting Rotary Switch, 2 Pole, 8 Position, 15 A at 5 V	Centralab	JV9033
7	1	Chassis	15" x 17" x 6" Chassis	Bud	AC1429
8	1	Line Cord	Line Cord, 6 ft.		
9	1	F1	Fuseholder and 2 A Fuse		HKP/AGC2A
10	1	K1	Relay, DPDT, 10 A, 120 VAC Coil	P & B	KRP11AG
11	1	XK1	Socket, Octal (for K1)		
12	1	S3	Switch, 3PST, 10 A at 120 VAC	Cutler-Hammer	7590K73C27
13	1	T1	Transformer	Hazeltine	3DTD893042

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Figure 3-3. Five-Volt Regulator Test Jig (Sheet 2 of 2)



7704066

Figure 3-4. Test Setup Diagram

4. Set overvoltage threshold potentiometer R18 fully clockwise and overcurrent potentiometer R19 fully counterclockwise.

3.2.2.2 Checkout Procedure. Perform the entire procedure to check out and align the unit after repair. For troubleshooting, omit those adjustments unrelated to the fault.

a. Adjustment Range

1. Set the test jig POWER switch to ON and adjust the variable transformer for an 11.0 ± 0.5 vac indication across jacks AC1/CT1 and across AC2/CT2.

2. Adjust 5V ADJ potentiometer R8 over its entire range and note that the indication at the DVM jacks varies from 4.95 vdc or less to 5.45 vdc or greater.

b. Load Regulation

1. Adjust variable transformer for 10.5 ± 0.1 vac across AC1/CT1 and across AC2/CT2.

2. Adjust R8 for 5.20 ± 0.25 vdc at the DVM jacks.

3. Set the LOAD SELECT switch to 3.0 A and note that the dc voltage does not change by more than ± 0.042 vdc.

4. Set the LOAD SELECT switch to NO LOAD.

5. Adjust variable transformer for 11.5 ± 0.1 vac across AC1/CT1 and across AC2/CT2.

6. Adjust R8 for 5.20 ± 0.25 vdc at the DVM jacks.

7. Set the LOAD SELECT switch to 3.0 A. Check that the dc voltage does not change by more than ± 0.042 vdc.

c. Line Regulation

1. Adjust R8 for 5.20 ± 0.25 vdc at the DVM jacks.

2. Adjust variable transformer to vary the voltage across AC1/CT1 from 10.50 vac to 11.50 vac and check that the output voltage does not vary by more than 0.008 vdc.

d. Ripple

1. Adjust the variable transformer for 11.0 ± 0.5 vac across AC1/CT1 and across AC2/CT2.

2. Set the LOAD SELECT switch to 3.0 A.

3. Adjust R8 for 5.20 ± 0.25 vdc across the DVM jacks.

4. Connect an oscilloscope across the SCOPE jacks, ac coupled, with vertical sensitivity set for 5 mV/cm.

5. Adjust variable transformer to vary the voltage at AC1/CT1 from 10.50 vac to 11.50 vac. Check that ripple does not exceed 5 mV peak-to-peak at any point.

e. Overvoltage Threshold Adjustment

1. Set the LOAD SELECT switch to NO LOAD and the TEST MODE switch to OVP SET.

2. Connect a dc power supply across the PWR SUPPLY terminals and set it for a 6.0 vdc indication across the DVM terminals.

3. Turn overvoltage threshold potentiometer R18 slowly counterclockwise until the dc voltage indication just drops.

4. Set the dc power supply for 0 volt output and turn its ac power switch off and then on (or disconnect and reconnect power cord if power supply has no switch).

5. Slowly increase the dc power supply output while watching the DVM. Check that the voltage rises to 6.0 ± 0.1 vdc and then drops.

6. Repeat step 4.

f. Foldback Adjustment

1. Set the TEST MODE switch to TEST and the LOAD SELECTOR switch to NORM LOAD.

2. Adjust the variable transformer for 11.0 ± 0.5 vac across AC1/CT1 and across AC2/CT2.

3. Connect an ammeter across the AMMETER jacks. The indication should be 3.6 ± 0.1 amps dc.

4. Turn foldback adjust potentiometer R19 slowly clockwise until the current just drops to 3.4 ± 0.1 amps.

5. Set R8 fully clockwise.

6. Set the LOAD SELECT switch to NO LOAD and then back to NORM LOAD. The overcurrent trip should no longer be activated.

7. Turn R8 slowly counterclockwise while watching the ammeter. The current should rise to 3.6 ± 0.1 amp dc, then drop slightly.

8. Repeat steps 5 and 6.

g. Final Voltage Setting

1. Adjust the variable transformer for 11.0 ± 0.5 vac across AC1/CT1 and across AC2/CT2.

2. Set the LOAD SELECT switch to 3.0 A.

3. Adjust R8 for a 5.20 vdc indication at the DVM jacks.

h. Hard Turn On

1. Set the variable transformer for 11.5 vac across AC1/CT1.

2. Set the POWER switch off and on several times. Check that the voltage at the DVM jacks returns to 5.20 ± 0.25 vdc each time power is turned on.

3. Set the LOAD SELECT switch to NO LOAD and repeat step 2.

3.2.2.3 RTV application. After all tests and adjustments are completed, apply a drop of fast curing RTV on R18 and R19.

3.3 TROUBLESHOOTING

3.3.1 Monitor Electronics Chassis (figure B-4)

The setup and procedure given in paragraph 3.2.1 may be used when troubleshooting the monitor electronics chassis. Table 3-2 is a troubleshooting chart, and tables 3-3 and 3-4 provide voltage and waveform data for use in troubleshooting the monitor electronics. A spare flyback transformer may be substituted without disassembly. Connect P5 to J5 on the circuit board, flying lead connector J7 to P7, and connect the CRT anode lead.

3.3.2 Five Volt Regulator (figure B-3)

The setup and procedure given in paragraph 3.2.2 may be used when troubleshooting the regulator. Table 3-1 lists normal voltage and resistance values at key points. The resistance values are for a regulator with no input or output connections. Voltages are given for normal operating conditions.

3.4 REPAIR AND REPLACEMENT

WARNING

Hazardous voltage may remain present in the CRT anode circuit after power is removed, and must be discharged before working on the CRT or monitor circuit board. Disconnect the anode lead from the side of the tube and use a screwdriver to ground it to the chassis.

All components of the monitor, and of the 5-volt regulator are directly accessible. Refer to Appendix A for part numbers of components not readily available. When replacing the flyback transformer, discard the shipping bracket and two nuts supplied. Use the nuts removed from the transformer replaced. Apply lock-tite to the threads and torque to 5 ±1 inch pounds. When replacing chassis-mounted transistors, apply a thin film of thermal compound, Hazeltine part number 1DTD460003, to the mating chassis and transistor surfaces.

Table 3-1. Voltage and Resistance Data for 5 Volt Regulator

<u>TEST POINTS</u> <u>(+), (-)</u>	<u>NORMAL VALUE</u>
CR3-1, E2	5000 ohms
E2, CR3-1	3000 ohms initially, >10 K after C6 charges
CR3-3, E2	5000 ohms
E2, CR3-3	3000 ohms initially, >10 K after C6 charges
E4, E5	600 ohms
A1-1, E5	5.2 ±0.25 vdc
A1-2, A1-3	<0.1 vdc
A1-4, A1-5	6.8 to 7.5 vdc
A1-7 & 8, A1-5	7.9 vdc
A1-9, A1-5	7.9 vdc
A1-6, A1-10	6.7 vdc

Table 3-2. Monitor Troubleshooting Chart

<u>SYMPTOM</u>	<u>POSSIBLE REMEDY</u>
1. No picture, no raster	Check F2, Q7, Q2, Q5. If filaments are lit, Q2 is operational.
2. No video	Check Q10
3. Picture tears	Check Q13, U1
4. Picture rolls	Check Q14, Q3
5. Bright horizontal line	Check Q3, Q4, Q5
6. Very bright picture; contrast control has no effect	Check Q10, Q11

Table 3-3. Monitor Voltage and Waveform Data (Transistors)

REF DES	FUNCTION	BASE	EMITTER	COLLECTOR
Q1	Horiz drive	Waveform A	0 vdc	Waveform B
Q2	Horiz output	Waveform C	0 vdc	Waveform D
Q3	Vert oscillator	(GATE) Similar to Waveform N	(CATHODE) +1.2 vdc	(ANODE) Waveform E
Q4	Vert drive	Waveform E	Waveform F	+12 vdc
Q5	Vert output	Waveform F	Same as Waveform F except baseline is 0.7 V lower	Waveform G
Q6	Vert blanking	Similar to Waveform G, less amplitude	0 vdc	Waveform H
Q7	Series regulator	+72 vdc	+71 vdc	Waveform I
Q8	Pwr supply driver	+73 vdc	+72 vdc	+100 vdc similar to Waveform I
Q9	Pwr supply pre-driver	+16 vdc	+15 vdc	+73 vdc
Q10	Video output	+6.2 vdc	+5.6 vdc	Waveform J
Q11	Video	Input video	Waveform K	+5.6 vdc
Q13	Horiz buffer	Waveform L	0 vdc	Waveform M
Q14	Vert buffer	Waveform N	Waveform O	Waveform P

Table 3-4. Monitor Voltage and Waveform Data (Microcircuits and CRT)

REF DES	FUNCTION	PIN NUMBER			
		1	2	3	4
U1	Horiz Oscillator	1 Waveform A	2 0 vdc	3 Waveform M	4 Waveform Q
		5 +3.2 vdc	6 +8.4 vdc	7 Waveform R	8 +3.6 vdc
U2	Pwr Supply ampl	1 No conn	2 +6.2 vdc	3 +6.2 vdc	4 0 vdc
		5 No conn	6 +16 vdc	7 +30 vdc	8 No conn
P6	CRT socket	1 0 vdc	2 Waveform S (variable dc level)	3 5.20 vdc	4 Waveform T
		5 0 vdc	6 Same as Pin 2	7 Waveform U	8 Waveform V

NOTE: See figure 3-2 for waveforms

SECTION 4

FACTORY MAINTENANCE

4.1 INTRODUCTION

4.1.1 Scope

This section covers checkout and repair of the keyboard/logic assembly and checkout of a complete terminal after repair. Maintenance of the 5-volt regulator and the monitor are covered in Section 3. Refer to Appendix A for recommended spare parts, and to Appendix B for schematic diagrams.

4.1.2 Test Equipment

The following items of test equipment, or equivalent, are required for factory maintenance:

<u>Equipment</u>	<u>Manufacturer</u>	<u>Part Number</u>
Oscilloscope	Tektronix	465
Frequency Counter	Hewlett Packard	5300A/5302A
Automatic Card Tester	Fairchild Technology Systems	Century 200
Hot Mock-up Test Bed	Hazeltine Corp.	
Interface Fixture	Hazeltine Corp.	1E-22973
Master Video Display Terminal	Hazeltine Corp.	Modular One, modified for Type I turn-on and U/L case display
Printer	Hazeltine Corp.	Thermal Printer

The hot mock-up test bed is a model 1520 terminal with a transparent size/centering overlay as shown in figure 3-1.

4.2 CHECKOUT

4.2.1 General

The following procedure may be used to check out the keyboard/logic assembly after repair, or to check out a complete terminal. Connect the keyboard/logic assembly to be tested in a hot mock-up test bed.

4.2.2 Setup and Preliminary Adjustments

1. Make the following preliminary settings:

		1510/1520 only	
<u>Switch</u>	<u>Position</u>	<u>Switch</u>	<u>Position</u>
BAUD RATE	9600	ESCAPE/~	~
PARITY	EVEN	FORMAT	Off
HALF DUP/FULL	HALF DUP	EOM A & B	OFF
AUTO LF/CR	AUTO LF	WRAPAROUND	YES
U/L CASE/UP	U/L CASE		
STD VID/REV	STD VID		
EIA/CUR LOOP	EIA (2 switches)		

WARNING

Dangerous voltages (15 K vdc and 115 vac) are present in the terminal, and high voltage may be retained in the monitor circuits after power is removed. Exercise caution when working within the unit.

2. Connect the power plug to a 115 volt 60 Hz source and set the power switch to on.
3. Check that the POWER ON LED is on.
4. Check the voltage between the following points and E1 (ground terminal adjacent to J101).

<u>'202..</u> <u>board</u>	<u>'246 test</u> <u>connector</u>	<u>Voltage</u>
U48-22	-29	-12.0 ±0.2 vdc
U48-23	-3	+12.0 ±0.2 vdc
U48-24	-4	-5.0 ±0.2 vdc
C68(+)	-20 & -21	+5.2 ±0.25 vdc

5. Type four full rows of characters evenly spaced from the top to the bottom of the display.
6. Adjust the monitor BRIGHT control R26 until the raster is just visible.
7. If necessary, touch up the monitor HORIZ HOLD, R5; VERT SIZE, R36; and WIDTH, R57 to obtain proper size and synchronization.

8. Verify that the display can be adjusted for proper size and centering as described in paragraph 3.2.1.2.
9. Adjust BRIGHT control R26 until the raster just disappears.
10. Set the power switch of off.

4.2.3 Interface tests

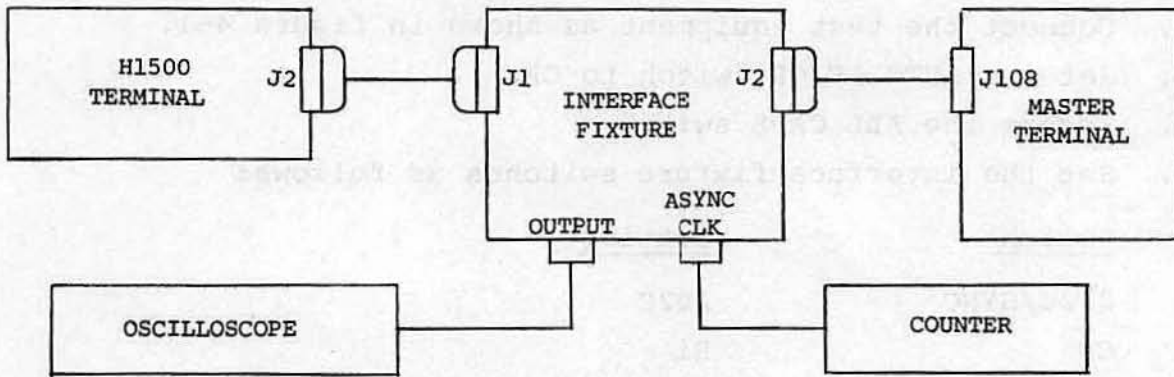
1. Connect the test equipment as shown in figure 4-1.
2. Set the AUTO LF/CR switch to CR.
3. Engage the ALL CAPS switch.
4. Set the interface fixture switches as follows:

<u>Switch</u>	<u>Setting</u>
202C/SYNC	202C
CB	Hi
CC	Hi
CF	Hi
Current Loop	Off

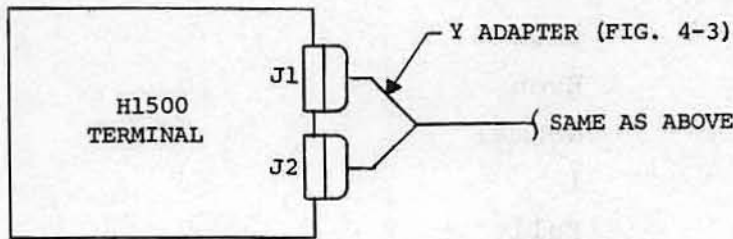
5. Set the master terminal controls as follows:

<u>Switch</u>	<u>Setting</u>
Baud Rate	9600
Parity	Even
Video	Normal
Stop Bits	1
Duplex	Full
LF/CR Auto	Disable
U/C Only	Disable
Power	On

6. The checkout procedure follows in tabular format. Perform the actions listed in the first two columns for the unit under test and the master terminal. Check that the results listed in the third and fourth columns of the table occur. Use of the control and/or shift keys is indicated by a superscript "c" or "s" preceding the character. Thus, ^{CS}A requires striking the A key while holding the CTRL and SHIFT keys down. Spaces between keystrokes in the table are included for clarity; they have no significance and are not to be typed. When a space is required it is spelled out.



a. INTERFACE TEST SETUP



b. AUXILIARY OUTPUT TEST SETUP

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Figure 4-1. Test Equipment Setup

ACTION		RESULT	
UNIT UNDER TEST (UUT)	MASTER TERMINAL	UNIT UNDER TEST	MASTER TERMINAL
Power on		POWER ON LED on Screen clear Cursor home Video synchronized within 1 minute	
Enter: 1 2 3 4 5 6 7 8 9 0 - \		1 2 3 4 5 6 7 8 9 0 - \ appear on screen	1 2 3 4 5 6 7 8 9 0 - \ appear on screen
HALF DUP/FULL to FULL Enter: QWERTYUIOP@[-		No change	QWERTYUIOP@[- appear on screen
HALF DUP/FULL switch to HALF Depress and hold the A key until more than 80 A characters are entered		Continuous stream of A's, continued on second line when end of first line is reached	Same as UUT
Depress: RETURN		Cursor returns to first character position of present line. Cursor blinks (display alternates between character and cursor)	
Enter: ASDFGHJKL;:]		ASDFGHJKL;:] appear on screen	Same as UUT
Enter: LINE FEED		Cursor moves down one row but maintains character position	Same as UUT
Set AUTO LF/CR to AUTO LF Enter: ZXCVBNM,./		ZXCVBNM,./ appear on screen	Same as UUT
Enter: RETURN		Cursor moves to start of next line	Cursor moves to start of present line
Enter additional RETURN's until scrolling starts. Using the numeric cluster, enter: 0,.123456789		0,.123456789 appear on bottom row of screen	0,.123456789 appear on screen
Enter: RETURN		Display moves up one row. Cursor moves to first character position of bottom row. Bottom row is clear.	
Enter: LINE FEED		No cursor movement	
Disengage ALL CAPS key. AUTO LF/CR to CR Enter: QWERTYUIOP		Lower case qwertyuiop appear on screen	Same as UUT
Enter: LINE FEED		Scrolling occurs; cursor maintains character position	No change

ACTION		RESULT	
UNIT UNDER TEST (UUT)	MASTER TERMINAL	UNIT UNDER TEST	MASTER TERMINAL
Enter: RETURN		Cursor moves to first character position. No scrolling occurs.	Cursor moves to start of next row
AUTO LF/CR to AUTO LF Enter: ASDFGHJKLZXCVBNM		Lower case asdfghjklzxcvbnm appear on screen	Same as UUT
With the left SHIFT key depressed, enter: ! "\$ % & / () = ~ ! ;		! "\$ % & / () = ! appear on screen	! "\$ % & / () = ! appear on screen
With the right SHIFT key depressed, enter: QWERTYUIOP { ASDFGHJKL+* } ZXCVBNM<>?		QWERTYUIOP { ADFGHJKL+* } ZXCVBNM<>? appear on screen	QWERTYUIOP { ASDFGHJKL+* } ZXCVBNM<>? appear on screen
U/L CASE/UP to UP	Press each alpha and numeric key	Upper case alpha characters, and numbers appear on screen	-
	Depress SHIFT and each alpha and numeric key	Upper case alpha characters and symbols as marked over numeric keys on master are displayed	-
Press each alpha key		Upper case characters appear on screen	Same as UUT
U/L CASE/UP to U/L CASE Engage ALL CAPS key	Enter some random alpha characters	Upper case characters appear on screen	-
Depress and hold the A key		A's appear on screen	Same as UUT
Depress and hold the S key without releasing the A key		No change	
Release the A key		S's appear on screen	Same as UUT
Sequentially depress and hold the A S and D keys.		A's appear on screen S's appear on screen D's appear on screen	Same as UUT
Release the A key			
Release the S key			
Release the D key			
Depress: CLEAR		Screen clears, cursor homes	No change
AUTO LF/CR to CR Enter: 1 2 RETURN LINE FEED 3		1 2 3 appear on screen	Same as UUT

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ACTION		RESULT	
UNIT UNDER TEST (UUT)	MASTER TERMINAL	UNIT UNDER TEST	MASTER TERMINAL
Enter: BACK SPACE		Cursor moves one position to left. Display is unchanged	Same as UUT
Enter: BACK SPACE		Cursor moves up one line and over to last column	Same as UUT
Enter: HOME		Cursor homes	No action
Enter: BACK SPACE		No action	Cursor moves one position to left
Enter: ^S BACK SPACE		Cursor moves right one position	No action
Enter: LINE FEED		Cursor moves down one line	No action
Enter: ^S LINE FEED		Cursor moves up one line	No action
Enter random characters on three full rows including the top and bottom rows. Position the cursor near the middle of the top row. Enter: ^C CLEAR.	Position the cursor near the middle of the top row	Data is cleared from cursor position thru end of top row	No action
Enter: ^{CS} CLEAR		Data is cleared from cursor position thru end of screen	No action
Enter random characters on the top and bottom rows. Move cursor to end of screen			
Enter: CLEAR		Entire screen is cleared	No action
HALF DUP/FULL to FULL			
Enter: 1 2 RETURN		No action	1 2
LINE FEED 3			3 appear on screen
Enter: BACK SPACE		Cursor moves left one position. Display is unchanged	Cursor moves left one position. Display is unchanged
Enter: BACK SPACE		No action	Cursor moves to last character position and up one line
Enter: HOME		No action	Cursor homes
Enter: LINE FEED		No action	Cursor moves down one line
Enter: ^S LINE FEED		No action	Cursor moves up one line
Enter: ^S _N ^C _O		No action	F8 indicator comes on
Enter: ^S _N ^C _X		No action	F8 indicator goes out

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ACTION		RESULT	
UNIT UNDER TEST (UUT)	MASTER TERMINAL	UNIT UNDER TEST	MASTER TERMINAL
Enter: ^S CLEAR	Enter FMAT mode and Half Duplex. Enter some foreground data on the screen. Exit FMAT and enter some background data	No action	Foreground data is cleared
Enter: CLEAR		No action	Entire screen is cleared
DISPLAY MEMORY TESTS			
HALF DUP/FULL TO HALF DUP BAUD to 9600 PARITY TO EVEN	Enter: HOME Fill screen with U's Move cursor to end of screen and press: SEND	Screen fills with U's except last character position in bottom row U appears, scrolling occurs	Screen fills with U's
Enter: ^S U and hold			
Repeat the above procedure except set the CHARACTER SELECT switch to *		Same as above except asterisks are displayed instead of U's	
RAM ADDRESS LINES AND REMOTE CURSOR ADDRESS CHECKS			
	Enter each of the following sequences: CLR UNPRO RESET ~ ^C Q ^C A ^C SPACE A ~ ^C Q ^C B ^C SPACE B ~ ^C Q ^C D ^C SPACE C ~ ^C Q ^C H ^C SPACE D ~ ^C Q ^C P ^C SPACE E ^C Q SPACE ^C SPACE F ~ ^C Q @ ^C SPACE G ~ ^C Q Ø A H ~ ^C Q ^C P C I ~ ^C Q SPACE F J ~ ^C Q ^C S O L K ~ ^C Q / L L ~ ^C Q 7 L M ~ ^C Q ; L N ~ ^C Q ^S = L O ~ ^C Q ^S > L P ~ ^C Q ^S ? L Q ~ ^C Q @ L R ~ ^C Q ^C O S S ~ ^C Q ^C S O V T ~ ^C Q O W	Note that none of the previous characters is affected as each character is displayed. A is displayed B is displayed C is displayed D is displayed E is displayed F is displayed G is displayed H is displayed I is displayed J is displayed K is displayed L is displayed M is displayed N is displayed O is displayed P is displayed Q is displayed R is displayed S is displayed T is displayed Cursor moves to line 24, column 80 screen should look like figure 4-2	

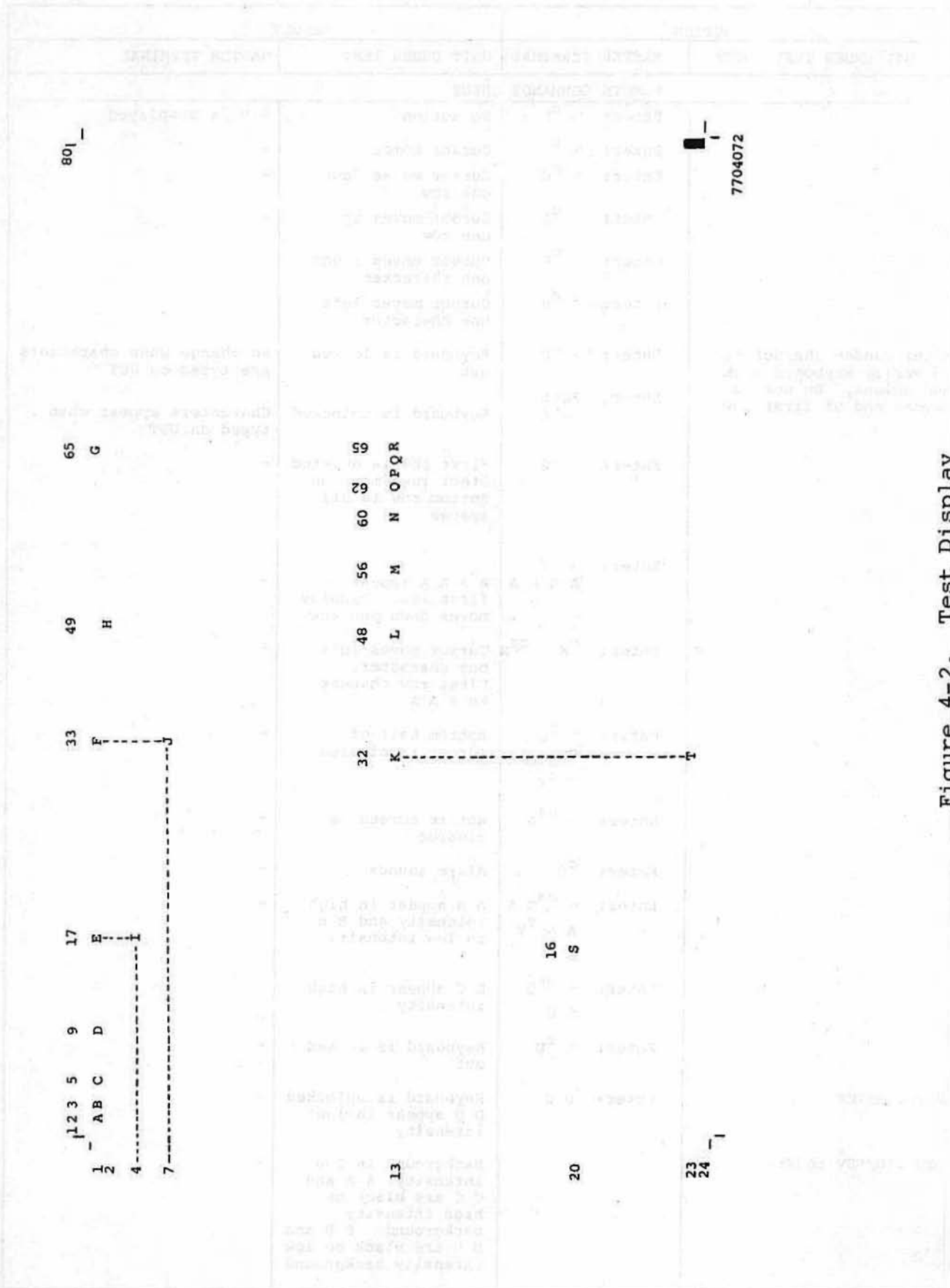
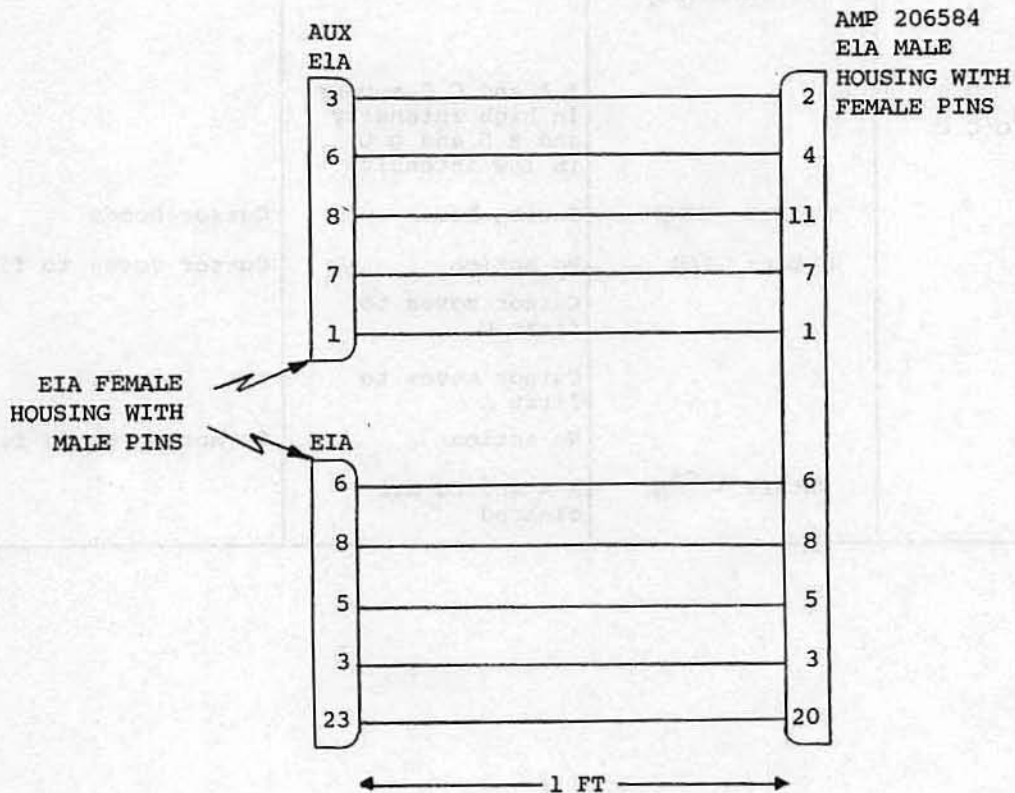


Figure 4-2. Test Display

ACTION		RESULT	
UNIT UNDER TEST (UUT)	MASTER TERMINAL	UNIT UNDER TEST	MASTER TERMINAL
<p>HALF DUP/FULL to FULL Enter: CLEAR</p> <p>HALF DUP/FULL to HALF DUP Enter: ^SCLEAR</p> <p>Enter: CLEAR ^S ^{CS} O A A ^S ^C Y B B ^S ^{CS} O C C ^S ^C Y D D</p> <p>Enter: HOME</p> <p>Enter: TAB</p> <p>Enter: TAB</p> <p>Enter: ^S ^S TAB</p>	<p>Using FMAT mode, enter some fore- ground data and some background data</p> <p>HOME cursor. Using FMAT mode, enter: A A in high intensity, B B in low in- tensity, C C in high and D D in low intensity</p> <p>Enter: HOME</p> <p>Enter: TAB</p> <p>Enter: [~] ^{CS} M</p>	<p>No change</p> <p>A A and C C are cleared</p> <p>A A and C C appear in high intensity and B B and D D in low intensity</p> <p>Cursor homes</p> <p>No action</p> <p>Cursor moves to first C</p> <p>Cursor moves to first A</p> <p>No action</p> <p>A A and CC are cleared</p>	<p>Screen is cleared</p> <p>No change</p> <p>Cursor homes</p> <p>Cursor moves to first C</p> <p>Cursor moves to first A</p>

4.2.4 Current Loop and Control Checks

1. Set the CB switch on the interface fixture to Low.
2. Type some random characters on the terminal under test and check that there is no response at the master terminal.
3. On the interface fixture, set the CB switch to Hi, and the Current Loop switch to 20 mA.
4. Set the EIA/CUR LOOP switches (2) on the unit under test to CUR LOOP.
5. Set the HALF DUP/FULL switch to FULL.
6. Type some random characters on the unit under test and check that they appear on the screen.



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Figure 4-3. Y Adapter Cable

4.2.5 Parity Checks

1. Set the Current Loop switch on the interface fixture to Off.
2. Set the HALF DUP/FULL switch on the unit under test to HALF DUP.
3. For each line below, set the parity switches on the unit under test and the master terminal as indicated, make the keyboard entries listed, and check for the proper results:

Parity Setting		Keyboard Entry		Result	
UUT	Master	UUT	Master	UUT	Master
EVEN	EVEN		T U	T U	
EVEN	ODD		T U	P _E P _E	
EVEN	ODD	T U			? ?
0	ODD	T U			T ?
0	EVEN	T U			? U
1	EVEN	T U			T ?
1	ODD	T U			? U
ODD	ODD	T U			T U
ODD	ODD		T U	T U	
ODD	EVEN		T U	P _E P _E	

4.2.6 Break Check

1. On the interface fixture, set the EIA Monitor switch to BA, and connect an oscilloscope to the Output jack.
2. Check that a 225 ±25 millisecond positive pulse appears each time the BREAK key is pressed, and the voltage goes from -10 ±2 volts to +10 ±2 volts.
3. Change the setting of the HALF DUP/FULL switch and repeat step 2.

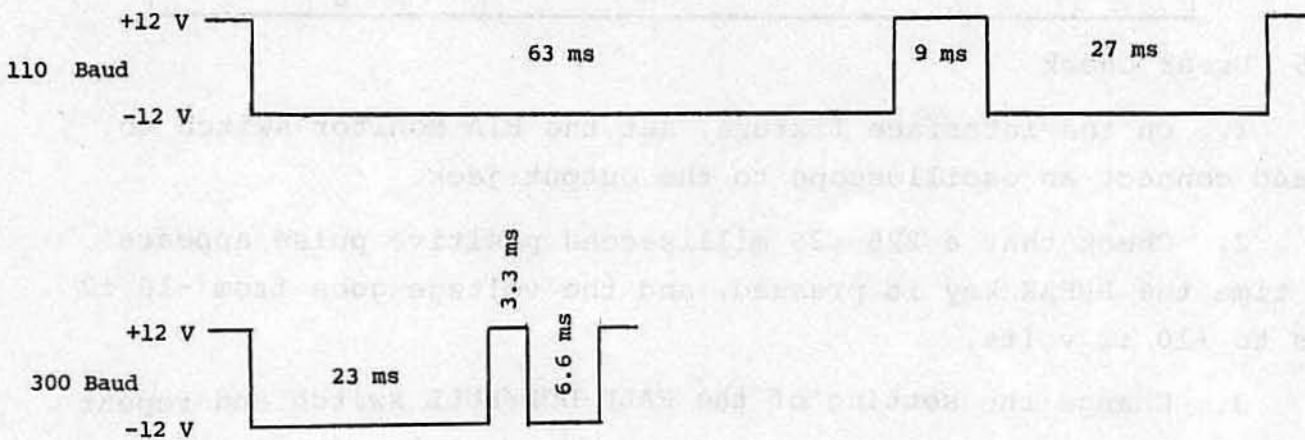
4.2.7 Baud Rate Checks

1. Set up the counter for frequency measurement.
2. Set each of the BAUD switches, one at a time, and check for the proper frequency indication:

<u>BAUD Switch</u>	<u>Frequency (KHz)</u>
19.2 K	302.592 to 311.808
9600	151.296 to 155.904
4800	75.648 to 77.952
2400	37.824 to 38.976
1800	28.368 to 29.239
1200	18.912 to 19.488
300	4.728 to 4.872
110	1.734 to 1.786

4.2.8 Stop Bits Check

1. Set the Scope Select switch on the interface fixture to BA.
2. Press and hold $S?$ and check for the 110 baud waveform as shown below.
3. Set the BAUD switches for 300 baud.
4. Press and hold $S?$ and check for the 300 baud waveform shown below.



4.2.9 Auxiliary Output Check

1. Connect a "Y" adapter cable (figure 4-3) as shown in figure 4-1(b).
2. Set the unit under test HALF DUP/FULL switch to FULL, and BAUD switches for 300 baud.

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3. Set the interface fixture CC and CF switches to Hi.
4. Set up the master terminal for Full Duplex operation and 300 baud.
5. Check that the CA, SA, and CD lights on the interface fixture are on.
6. Enter random characters on the unit under test and check that no characters appear on the master screen.
7. Enter some random characters on the master keyboard and check that they appear on the master screen and the CA, SA, and CD lights go on.
8. Set the unit under test BAUD switches for 1800.
9. Set the interface fixture CC and CF switches to Low. Check that the CA, SA, and CD lights are off.
10. Set the unit under test BAUD switches for 300.
11. Set the interface fixture CC and CF switches to Hi.
12. Type some random characters on the unit under test and check that they appear on the master screen.
13. Type some random characters on the master keyboard and check that they appear on the unit under test screen.

4.2.10 Format Mode and Printer Buffer Check (1510/1520 only).

1. Connect a thermal printer to the terminal PRINTER connector. Omit the printer and ignore steps concerning print functions if checking a 1510 terminal.

2. Set Switches as follows:

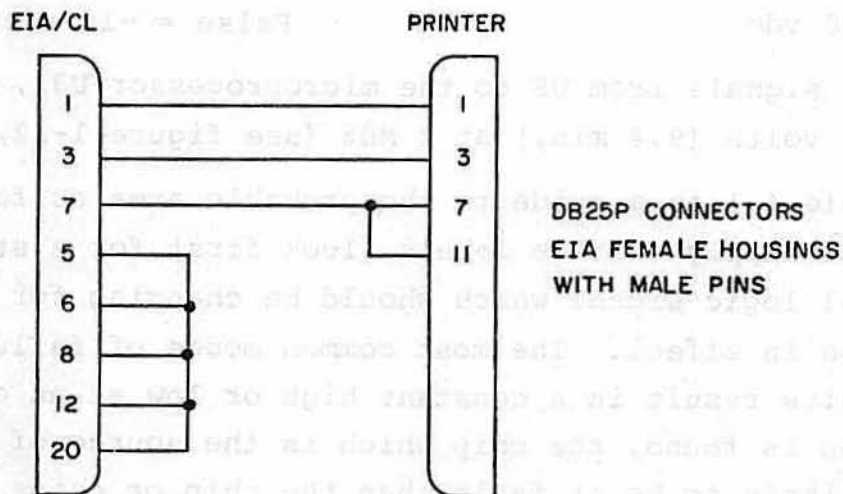
<u>Switch</u>	<u>Position</u>	<u>Switch</u>	<u>Position</u>
BAUD RATE	9600	ESCAPE/~	ESCAPE
PARITY	EVEN	FORMAT	Off
HALF DUP/FULL	HALF	EOM ^A _B	OFF
AUTO LF/CR	AUTO LF	WRAPAROUND	ON
U/L CASE/UP	U/L CASE	Printer Buffer	NO
EIA/CUR LOOP	EIA (2 switches)		S1-1, -2 & -3 Up

3. Set up the master terminal and interface fixture in accordance with paragraph 4.2.3 steps 4 and 5.

ACTION		RESULT	
UNIT UNDER TEST (UUT)	MASTER TERMINAL	UUT OR PRINTER	MASTER TERMINAL
Turn power on		POWER ON LED on Screen clear Cursor home	
Press and hold any character key		Characters appear until end of first row. Cursor stops at last position of first row.	Characters continue on second row.
	Enter: ESC - (hyphen)	No change	! appears on screen (followed by EOT which may be displayed as ^D)
	Enter: ESC # ESC ^L	FORMAT LED on Screen clears Cursor homes	
WRAPAROUND to YES Enter: QWerty... ...Y		QWERTY...appears in foreground intensity and wraparound occurs.	No change
	Enter: ESC ^N	! appears at cursor position. Cursor moves to next line.	QWerty...appears on screen
	Enter: ESC ^N	!! appears at cursor position. QWERTY... ...Y is printed.	No change
	Enter ESC - (hyphen)	No change) appears (followed by EOT which may be displayed as ^D).
	Enter ESC /	Printer On-Line light comes on.	
Enter some random characters and press SEND		Characters are printed.	Characters are displayed
	Enter some random characters	Characters are displayed and printed. LOCAL LED is on.	
	Enter: ESC ?	Printer On-Line light goes out.	
Press RESET		LOCAL and FORMAT LEDs go out.	

4.2.11 Printer Buffer Serial Output Checks (1520 only).

1. Connect the PRINTER output connector to EIA/CL connector J2 with a cable as shown in figure 4-4.
2. Select 110 baud, zero parity, and FORMAT mode at the terminal and set the printer buffer switches as follows: S1-1 and S1-2, Up; S1-3, Down.
3. Turn power on and enter some random characters on the screen.
4. Press ^SPRINT. The print symbol should appear on the top line and the characters duplicated on the second line in background intensity.
5. Set printer buffer switch S1-2 down, and the terminal BAUD RATE switches for 300.
6. Press ^SPRINT. The second line should be repeated on line 3.
7. Set printer buffer switch S1-1 down, and the terminal BAUD RATE switches for 1200.
8. Press ^SPRINT. The third line should be repeated on line 4.



7801026

Figure 4-4. Serial Print Test Cable

4.3 TESTING AND TROUBLESHOOTING

4.3.1 Keyboard/Logic Assembly and Printer Buffer.

4.3.1.1 Test and troubleshoot the keyboard/logic assembly and the printer buffer using the Automatic Card Tester and the appropriate adapter and tape set.

4.3.1.2 The following guide is furnished as an aid to limited troubleshooting of the keyboard/logic assembly and printer buffer with a multimeter and oscilloscope, and should permit a technician with a thorough knowledge of the theory of operation to isolate the cause of a majority of logic failures. Reference designations are for the '246-() boards, with the '202 board designations in parentheses. The dc power distribution should be checked (figure 2-3) before logic circuit troubleshooting.

4.3.1.3 With two exceptions, all logic levels are positive T^2L :

Zero = 0.0 to 0.4 vdc

One = 2.4 to 5 vdc

The exceptions are:

a. EIA inputs at U58 (U54) and outputs from U70 (U65) in the serial I/O area and inputs to U1 and outputs from U2 on the printer buffer board:

Zero = +10 vdc Control Signals, True = +10 vdc

One = -10 vdc False = -10 vdc

b. Clock signals from U8 to the microprocessor U31, which are nominally 10 volts (9.4 min.) at 2 MHz (see figure 1-12).

4.3.1.4 Use table 4-1 as a guide to the probable area at fault. After checking dc supply voltage levels, look first for a steady high or low level logic signal which should be changing for the mode of operation in effect. The most common modes of failure in integrated circuits result in a constant high or low at an output. If this condition is found, the chip which is the source of the signal is more likely to be at fault than the chip or chips which receive the signal.

4.3.2 Monitor and 5-volt regulator

The monitor and 5-volt regulator are covered in Section 3.

4.4 ALIGNMENT

The keyboard/logic assembly and printer buffer require no alignment. Alignment of the monitor and the 5-volt regulator are covered in Section 3.

Table 4-1. Limited Troubleshooting Guide

GENERAL NOTES

1. Ref. designations are for '246-() boards with '202 board designations following in parentheses when different.
2. It is assumed that power distribution has been checked and fault has been isolated to the keyboard/logic assembly and/or printer buffer.
3. Simple faults which can be isolated from the schematic alone are not covered. Note that simple failures can result in major malfunctions (e.g. terminal in wrong mode due to selector switch failure or failure of a register).
4. The guide is limited to troubleshooting which can be performed with a multimeter and oscilloscope.

Trouble	Probable Cause	Remarks
<p>No video. POWER ON LED and monitor OK</p> <p>Display shakey, flashing or missing dots, or raster but no characters</p> <p style="text-align: center;"><u>NOTE</u></p> <p>Entering a stream of background ^SU characters (code 01010101) and foreground ^S* characters (code 10101010) will fully exercise all bits of the video module.</p>	<p>a. Video Module b. TV Synchronizer</p> <p>Video module</p>	<p>Type ^CG. Alarm should sound for 1/3 s. If missing, or excessively long or short, fault is probably in TV sync module (see fig. 1-10 and 1-11). Otherwise fault is probably in video module. Trace back from U71 (U75) with scope. Output from U71 should be 60 ns pulses at 3 v for foreground and 2 v for background</p> <p>Data from character generator U83 (U78) is loaded into U93 (U77) when S/L (pin 15 of U93 (U77) is low. When S/L goes high data is shifted out of U93 (U77) in parallel on leading edge of clock at pin 7. A full TV line of data is read into line buffer U63/U64 (U67/U57) via U66/U65 (U68/U58) when sync bus disable is low, and recirculated on the trailing edge of the LBC when sync bus disable is high. Faults confined to a particular line or lines (e.g. all characters display fault in third line) is characteristic of failure in character line counter area U84.</p>
<p>Wrong character on screen from keyboard</p> <p style="text-align: center;"><u>NOTE</u></p> <p>After turn-on, the top 12 lines, and the first 68 chars. on line 13 are stored in the low address block of memory U24-U31 (U22-U29) and the balance of the screen in U11-U18 (U9-U16). After scrolling begins the locations change.</p>	<p>a. Same error in char. transmitted: Keyboard Keyboard encoder</p> <p>b. Transmitted char. OK: Char. gen U83 (U78) Display memory</p>	<p>K/B encoder output is transferred to data bus when KBRDY U60 pin 4 (U55 pin 4) goes low. If fault is consistent over screen (e.g. keying B results in displaying A anywhere on screen) fault is probably in character generator. If fault is confined to certain display locations and moves when scrolling occurs, fault is probably in memory</p>

Table 4-1. Limited Troubleshooting Guide (Cont)

Trouble	Probable Cause	Remarks
Garbage characters on screen at turn on. Cannot clear.	<ul style="list-style-type: none"> a. Power distribution b. Display memory c. Microprocessor module d. Program memory 	<ul style="list-style-type: none"> a. Check dc voltage at pins listed in table 4-2 b. If characters scroll, fault is probably in memory (see note in preceding entry). c/d. Full isolation between ROM and microprocessor module is not practical without special equipment. However, peripheral causes can be eliminated. Check for presence of clock/timing signals (ref. to para. 4.3.1.3 b). Holding the RESET button down will keep the microprocessor and refresh address counter off the address and data busses to permit checking for shorts on the busses.
Constant reverse video or no reverse video	<ul style="list-style-type: none"> a. S2 b. Video module 	<ul style="list-style-type: none"> a. Pin 8 of test socket U38 (pin 10 of U35A) should be low for reverse video and high for normal video b. U92/U94 (U76/U80)
Display is foreground only or background only	<ul style="list-style-type: none"> a. Transmission of protected data only can be selected b. Transmission of protected data only cannot be selected 	<ul style="list-style-type: none"> a. Foreground/background bit not being latched by U62 (U56) b. U11/U24 (U9/U22)
Constant character window for entire display	Character generator	U83 (U78)
Vertical bars on screen. Cannot clear	Character generator	U83 (U78)
Some keyboard characters cannot be entered properly, others OK	<ul style="list-style-type: none"> Keyboard Keyboard encoder 	<p>If the problem characters have a common x or y coordinate, trace that signal. Scan is generated (x) at encoder U60 (U55) and returned (y) when key is depressed. If keyboard lockout occurs (holding a problem key down prevents entry of a character which can otherwise be keyed) fault is probably in the encoder.</p>
No cursor or video. Transmitted characters	<ul style="list-style-type: none"> TV synchronizer Refresh address counter Microprocessor module 	Refer to para. 1.3.7 and figs. 1-10 and 1-11
Display rolls. Data can be entered.	TV synchronizer	Check for vertical drive at J101-3

Table 4-1. Limited Troubleshooting Guide (Cont)

Trouble	Probable Cause	Remarks
No transmitted data or wrong data transmitted	Serial I/O module or interface	If data is displayed in full duplex with jumper (fig. 2-1 c) but not transmitted in half duplex, check clear-to-send (CB) and data set ready (CC) at J2-5 and -6. One of these inputs must be true (high) to enable half duplex transmission (ref. to para 4.3.1.3 a). If data cannot be transmitted in any mode, trace back the data signal (BA) from J2-2 (EIA) or J2-21/-25 (cur loop). Check baud rate (para. 4.2.7).
No received data or wrong data received	Serial I/O module	Trace received data (BB) from J2-3. Each input character should cause an RDA high at U54 (U49) pin 19. Character should be on data bus when RDE goes low at pin 4.
Wrong or missing characters in batch and/or page transmissions. Other transmissions OK.	RAM	U36, U37
PRINT function does not work. Data sent/received printed OK when printer is on-line	Microprocessor ROM Printer buffer memory	If printer rate is equal to or greater than the terminal baud rate, the printer buffer memory will not be required in on-line mode but will be used for PRINT function
Data sent/received not printed when printer is on line. PRINT function OK.	Interface	Check for printer on line signal high at U25 pin 2 of printer buffer
No data printed. Transmission & display OK	Printer buffer or interface	a. Serial Printer: Check serial printer busy false (high) at J1-49 (ref. para. 4.3.1.3 a). Check baud rate of output at J1-24. b. Parallel Printer: Check par printer busy false (low) at J1-25 and printer out of paper false (low) at J1-26

Table 4-2. DC Voltage Usage

+12 VDC				-12 VDC			
Ref. Des.		Type	Pin	Ref. Des.		Type	Pin
'246-()	'202			'246-()	'202		
U33	U31	8080	28	U63/U64	U57/U67	3409	12
U8	U8	8224	9	U54	U49	AY5-1013	2
U20	U18	8228	23*	U70/U48	U44/U65	MC1488	1
--	U78	MCM6570	3	U60	U55	AY5-3600	27
U45	U41	COM5016	9	-5 VDC			
Q1	Q1	2N2222	C**	U30	U31	8080	11
U81	U74	opto-iso.	5***	--	U78	MCM6570	1*
U70/U48	U65/U44	MC1488	14				

*via R17(R13) 1K
 **via R53(R43) 150
 ***via R92(R44) 5.6K

*-3 vdc via R45/R46

Table A-1. Spare Parts List

Ref Des	Usable On Code*	Hazeltine Part No.	Description	Level			
				Site Maint	Shop Maint	Factory/Depot	
				1-25	26-50		
Major Assemblies							
-		1DTD155213	CRT, Yoke and Video Filter	X	X	1	1
-	A,B	4DTD155215	5-V Regulator Assembly	X		1	2
-	C	4DTD155215-1	5-V Regulator Assembly	X		1	2
T1		1DTD702124	Power Transformer	X		1	2
-		3DTD155206	Switch Bracket Assembly	X			
-	A1	4DTD155202	Keyboard/Logic Assembly	X		1	2
-		or					
-	A2	4DTD155246-1	Keyboard/Logic Assembly	X		1	2
-	B,C	4DTD155246-2	Keyboard/Logic Assembly	X		1	2
-		4DTD155205	Monitor Chassis Assembly	X			
-	C	4DTD155251	Printer Buffer Board	X		1	2
-		1DTD702134	Video Filter	X		1	1
Components and Subassemblies/Monitor							
-		4DTD155192	Monitor Board		X	1	2
C26		1SPS271472	Capacitor		X		1
F2		1SPS430013-5	Fuse	X	X	5	5
T2		1DTD702108	Transformer		X	1	2
T3		1DTD702114	Flyback Transformer		X	1	1
U3		1SPS351845	Rectifier		X	1	2
Components/Chassis and Logic Board							
A1	A2, B, C						
-	-	1SPS431001	Circuit Breaker			1	2
U8	U8	1SPS912797	Clock Generator			1	2
U9-U16	U11-U18	1SPS910081-3	Memory			1	2
U22-U29	U24-U31						
U18	U20	1SPS712798	System Controller			1	2
U20	U22	1DTD702127	Program ROM			1	2
-	U23						
-	U36,U37	1SPS912781	RAM			1	2
U31	U33	1SPS910155	Microprocessor Unit			1	2
U39	U43	1SPS702129	Baud Rate PROM			1	2
U41	U45	1SPS912799	Baud Rate Generator			1	2
U49	U54	1SPS910802	UART			1	2
U44,U65	U48,U70	1SPS910071**	EIA Line Driver			1	2
U54	U58	1SPS910072***	EIA Line Receiver			1	2
U55	U60	1DTD702130	Keyboard Encoder			1	2
U71	U90	1DTD702128	Horizontal PROM			1	2
U78	-	1DTD702122	Character Generator			1	2
-	U83	1DTD702145	Character ROM			1	2
Components/Printer Buffer							
U5	C	1SPS912813	Microprocessor Unit			1	2
U9	C	1SPS912814	I/O Expander			1	2

*Usable on Codes

- A Model 1500
- A1 Keyboard/Logic Assembly 4DTD155202
- A2 Keyboard/Logic Assembly 4DTD155246-1
- B Model 1510
- C Model 1520

**Also U2 on Printer Buffer

***Also U1 on Printer Buffer

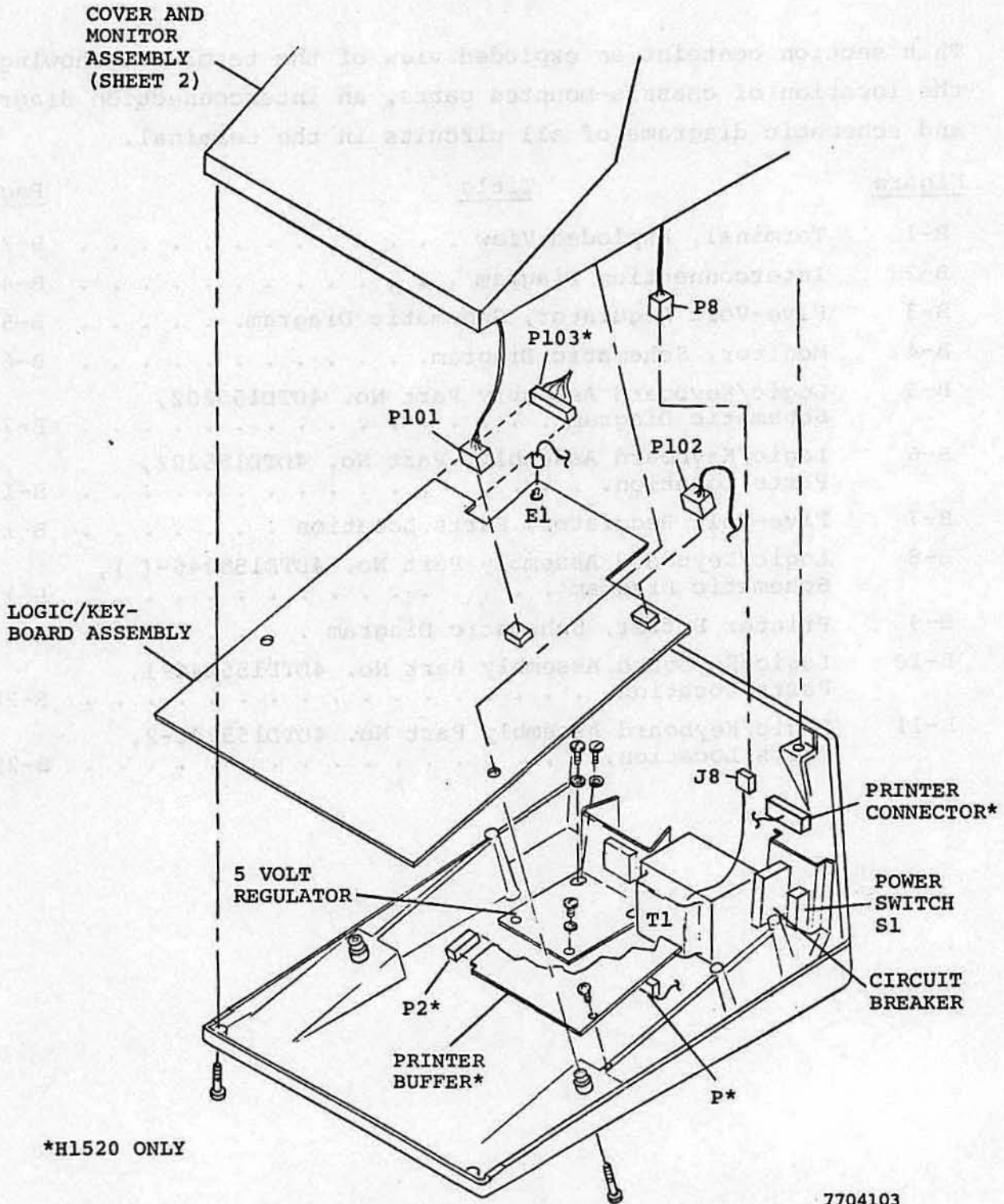
APPENDIX B

DIAGRAMS

This section contains an exploded view of the terminal, showing the location of chassis-mounted parts, an interconnection diagram, and schematic diagrams of all circuits in the terminal.

<u>Figure</u>	<u>Title</u>	<u>Page</u>
B-1	Terminal, Exploded View	B-2
B-2	Interconnection Diagram	B-4
B-3	Five-Volt Regulator, Schematic Diagram.	B-5
B-4	Monitor, Schematic Diagram.	B-6
B-5	Logic/Keyboard Assembly Part No. 4DTD155202, Schematic Diagram	B-7
B-6	Logic/Keyboard Assembly, Part No. 4DTD155202, Parts Location.	B-16
B-7	Five-Volt Regulator, Parts Location	B-17
B-8	Logic/Keyboard Assembly Part No. 4DTD155246-(), Schematic Diagram	B-18
B-9	Printer Buffer, Schematic Diagram	B-27
B-10	Logic/Keyboard Assembly Part No. 4DTD155246-1, Parts Location.	B-28
B-11	Logic/Keyboard Assembly Part No. 4DTD155246-2, Parts Location.	B-29

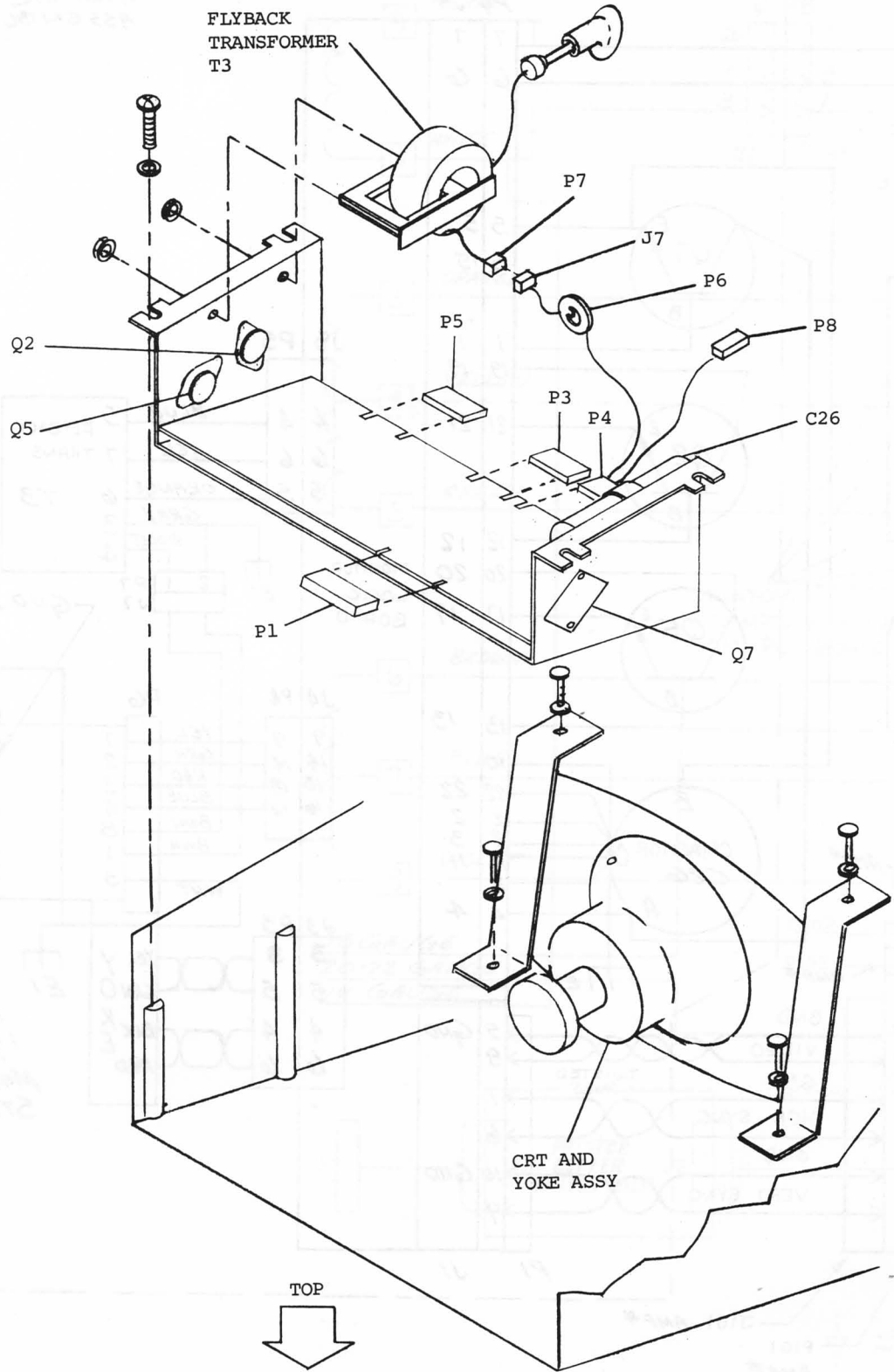
Figure B-1. Terminal, Exploded View (Sheet 1 of 5)



*H1520 ONLY

7704103

Figure B-1. Terminal, Exploded View (Sheet 1 of 2)



7704074

Figure B-1. Terminal, Exploded View (Sheet 2 of 2)

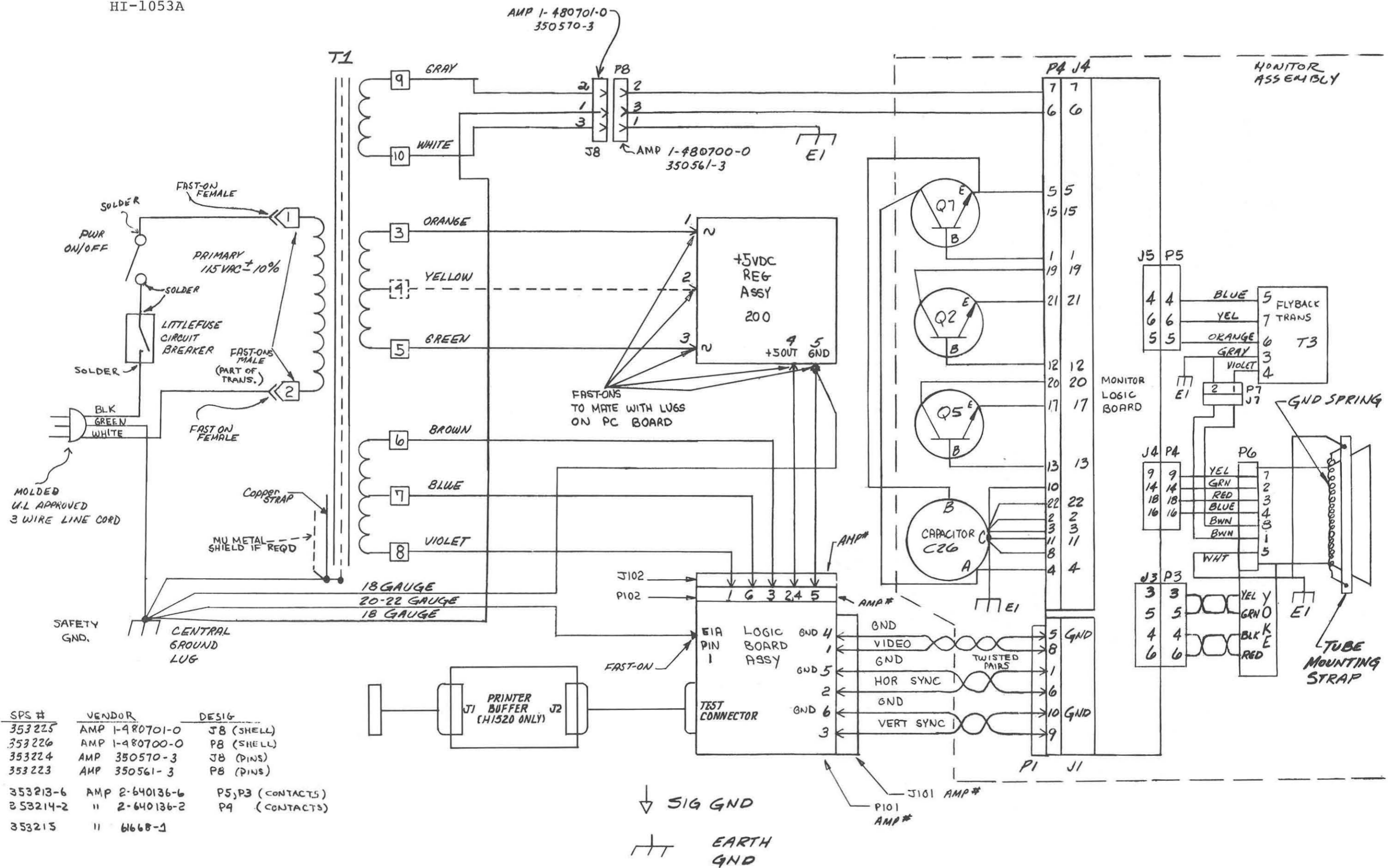
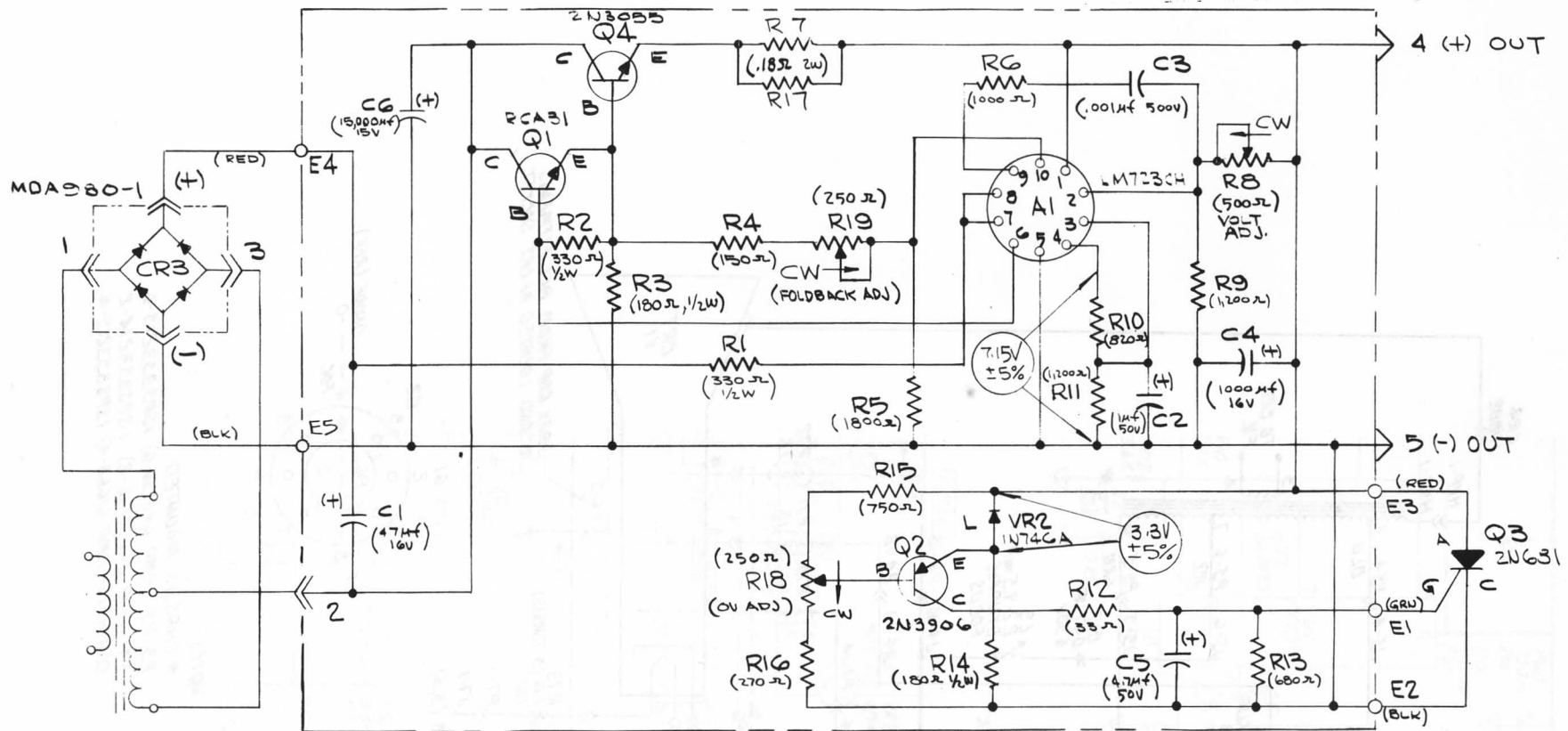
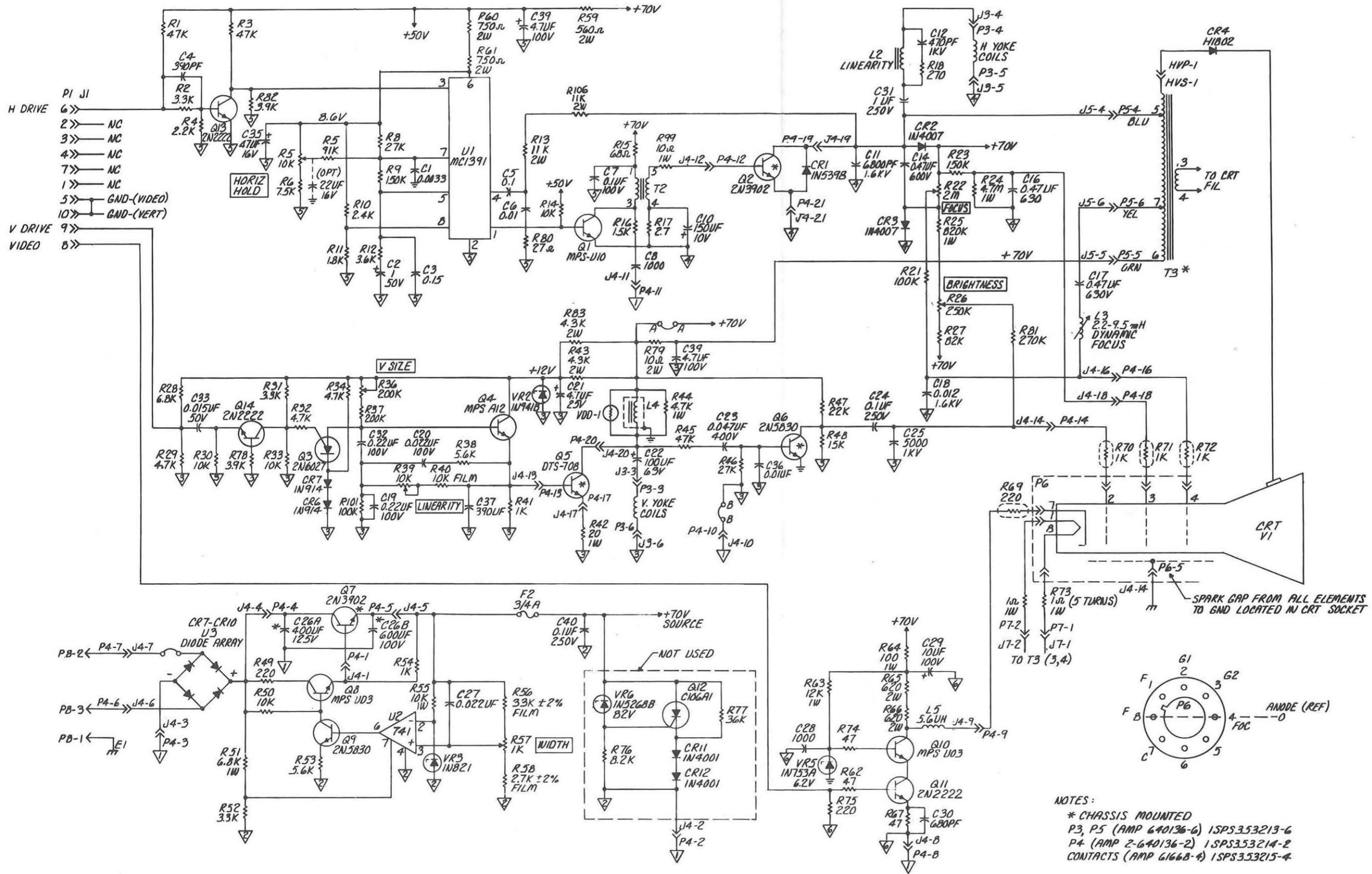


Figure B-2. Interconnection Diagram



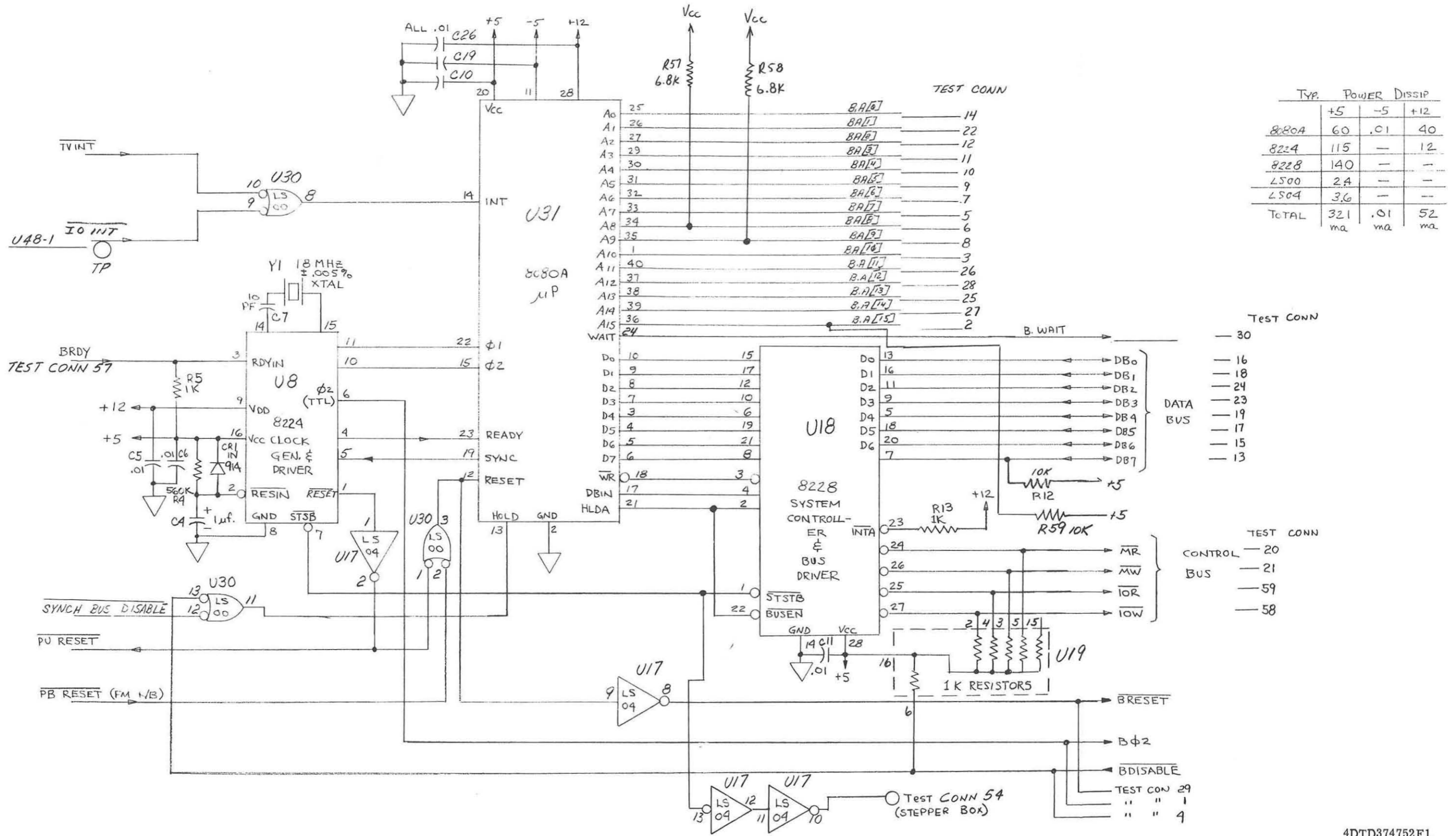
7704106

Figure B-3. +5 Volt Regulator, Schematic Diagram



NOTES:
 * CHASSIS MOUNTED
 P3, P5 (AMP 640136-6) 1SPS353213-6
 P4 (AMP 2-640136-2) 1SPS353214-2
 CONTACTS (AMP 61668-4) 1SPS353215-4

Figure B-4. Monitor Schematic Diagram



	TYP. POWER DISSIP		
	+5	-5	+12
8080A	60	.01	40
8224	115	—	12
8228	140	—	—
LS00	2.4	—	—
LS04	3.6	—	—
TOTAL	321 ma	.01 ma	52 ma

- TEST CONN
- 30
 - 16
 - 18
 - 24
 - 23
 - 19
 - 17
 - 15
 - 13
- DATA BUS
- TEST CONN
- 20
 - 21
 - 59
 - 58
- CONTROL BUS

4DTD374752F1

Figure B-5. Logic/Keyboard Assembly, Schematic Diagram (Sheet 1 of 9)

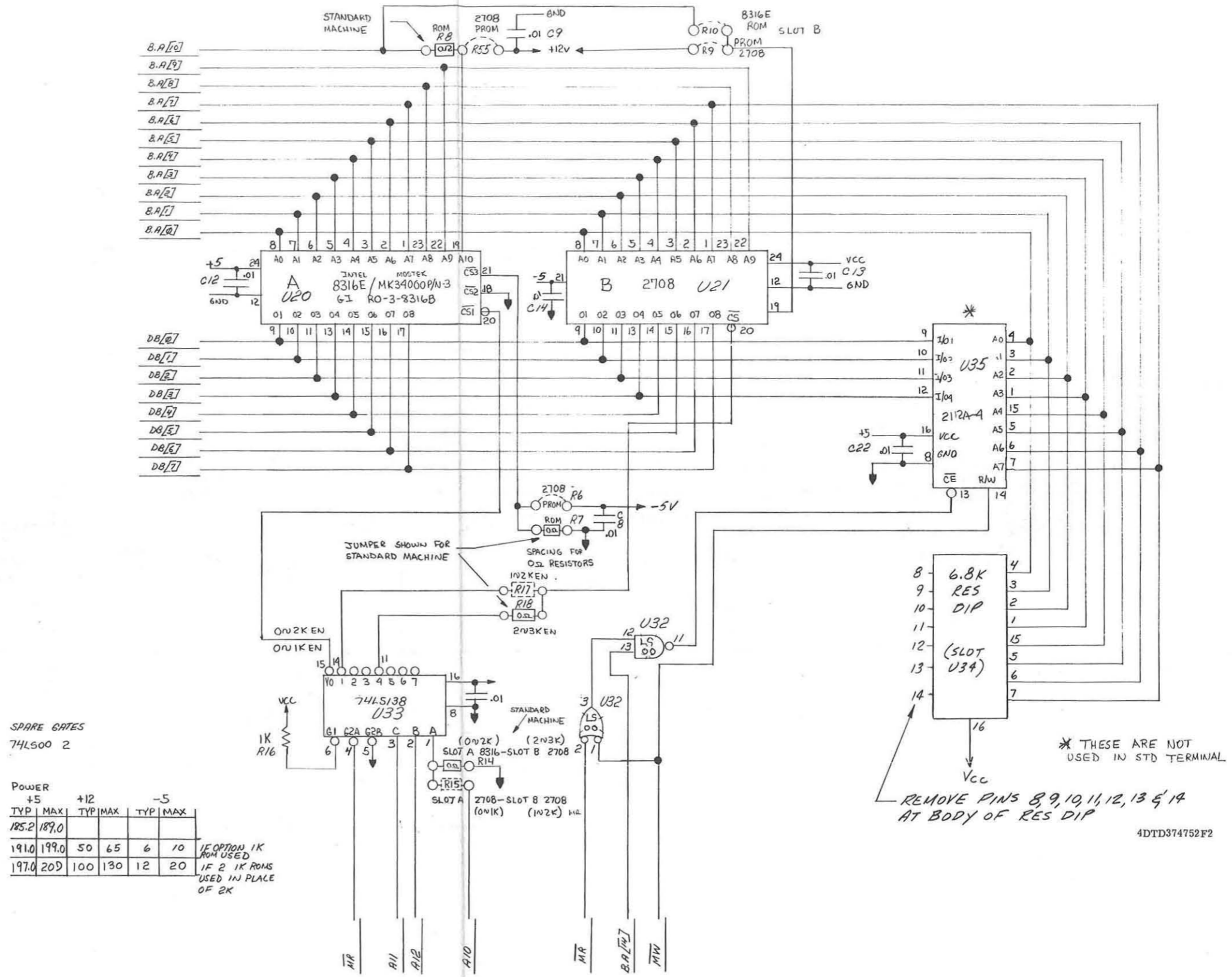


Figure B-5. Logic/Keyboard Assembly Schematic Diagram (Sheet 2 of 9)

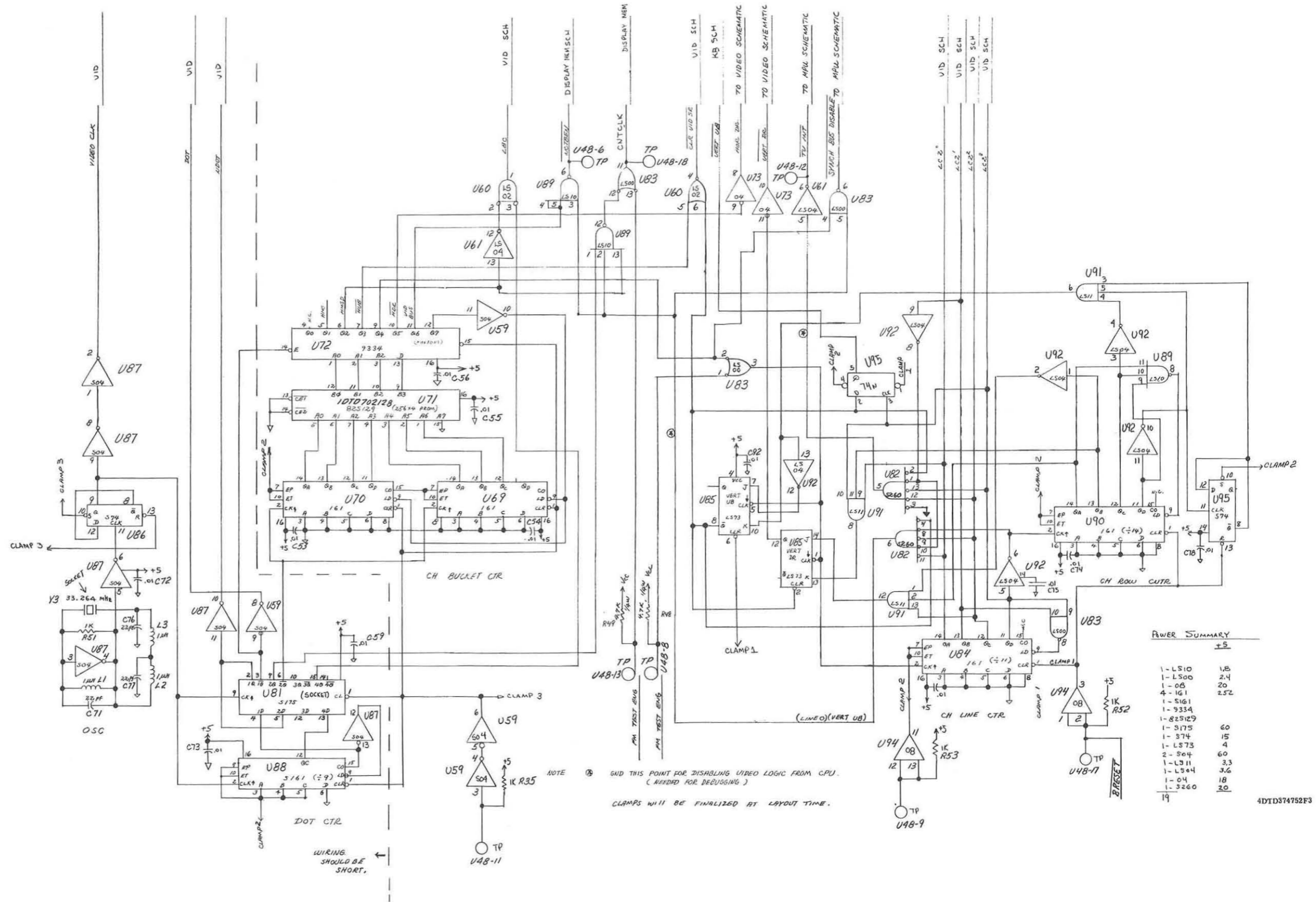


Figure B-5. Logic/Keyboard Assembly, Schematic Diagram (Sheet 3 of 9)

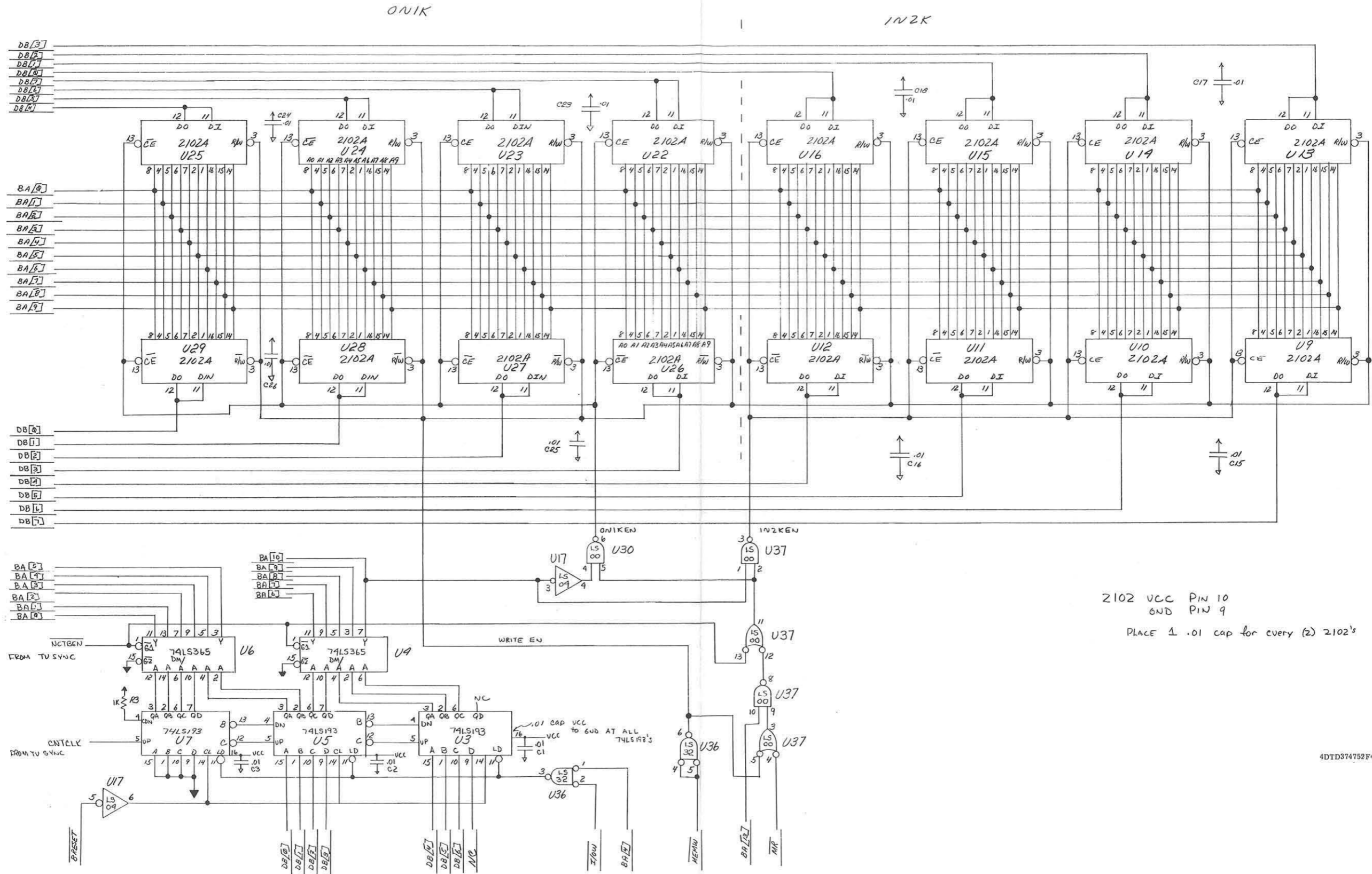
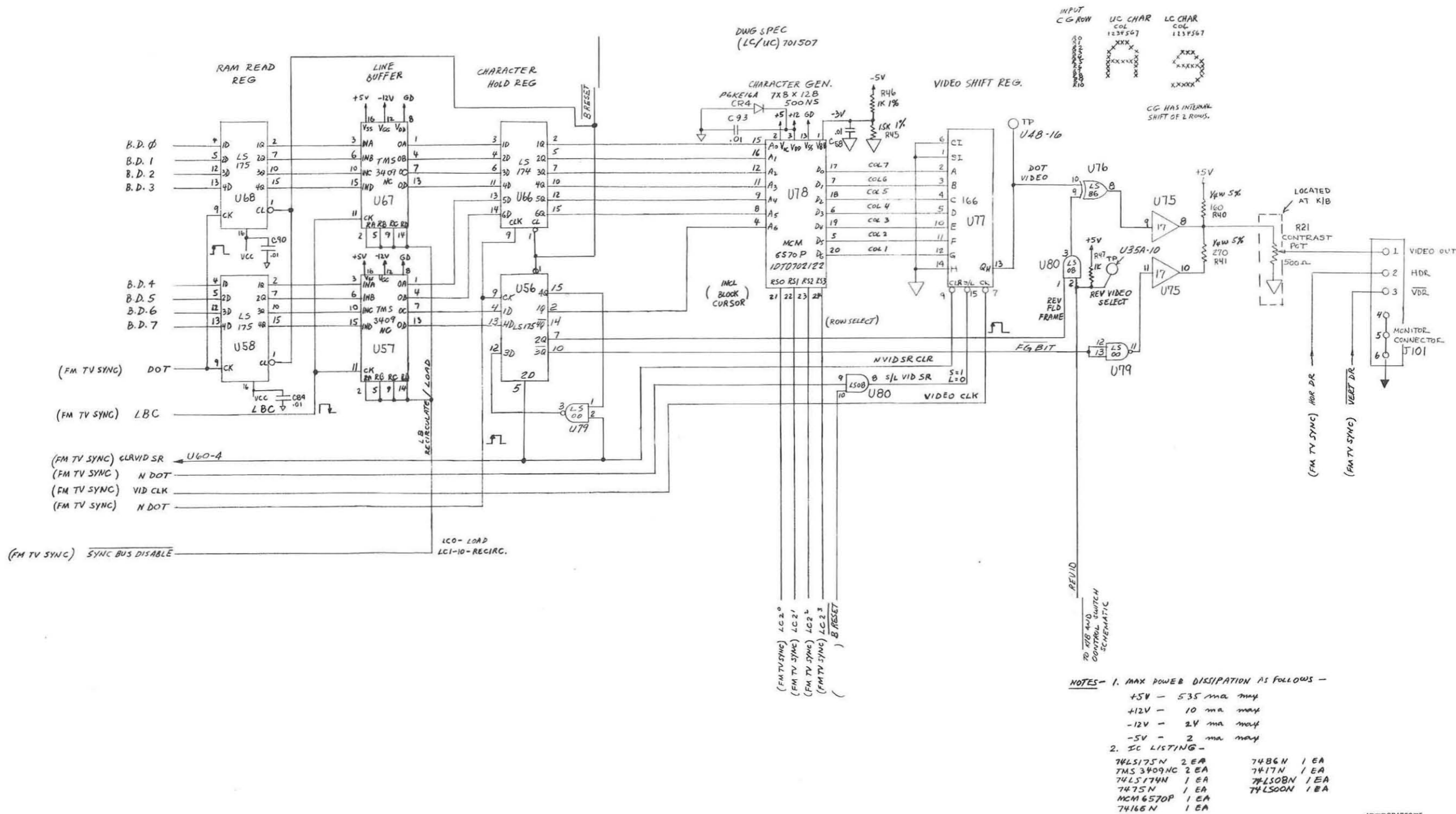
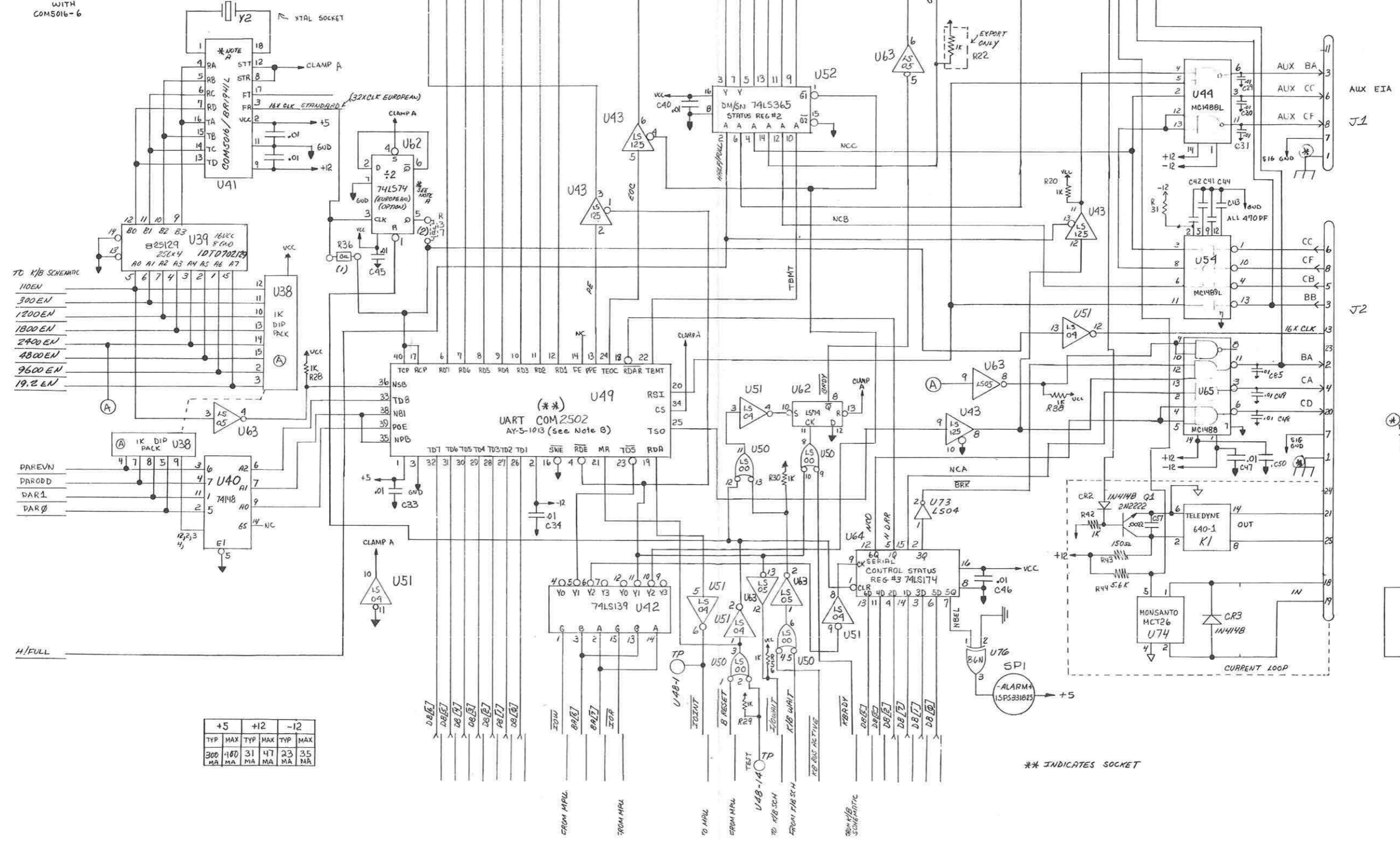


Figure B-5. Logic/Keyboard Assembly, Schematic Diagram
(Sheet 4 of 9)



NOTE A*
FOR EXPORT ONLY
1) REMOVE JUMPER (1)
2) REMOVE JUMPER (1)
3) INSERT JUMPER (2) (0.2 RESISTORS) 5.0688 MHZ AT CUT SERIES <math>Z < 50\Omega</math>
REPLACE COM5016/B1914L WITH COM5016-6



* INDICATES BOTH GND'S GO TO CHASSIS GND VIA MALE FAST-ON

** INDICATES SOCKET

4DTD374752F6

Figure B-5. Logic/Keyboard Assembly, Schematic Diagram (Sheet 6 of 9) B-12

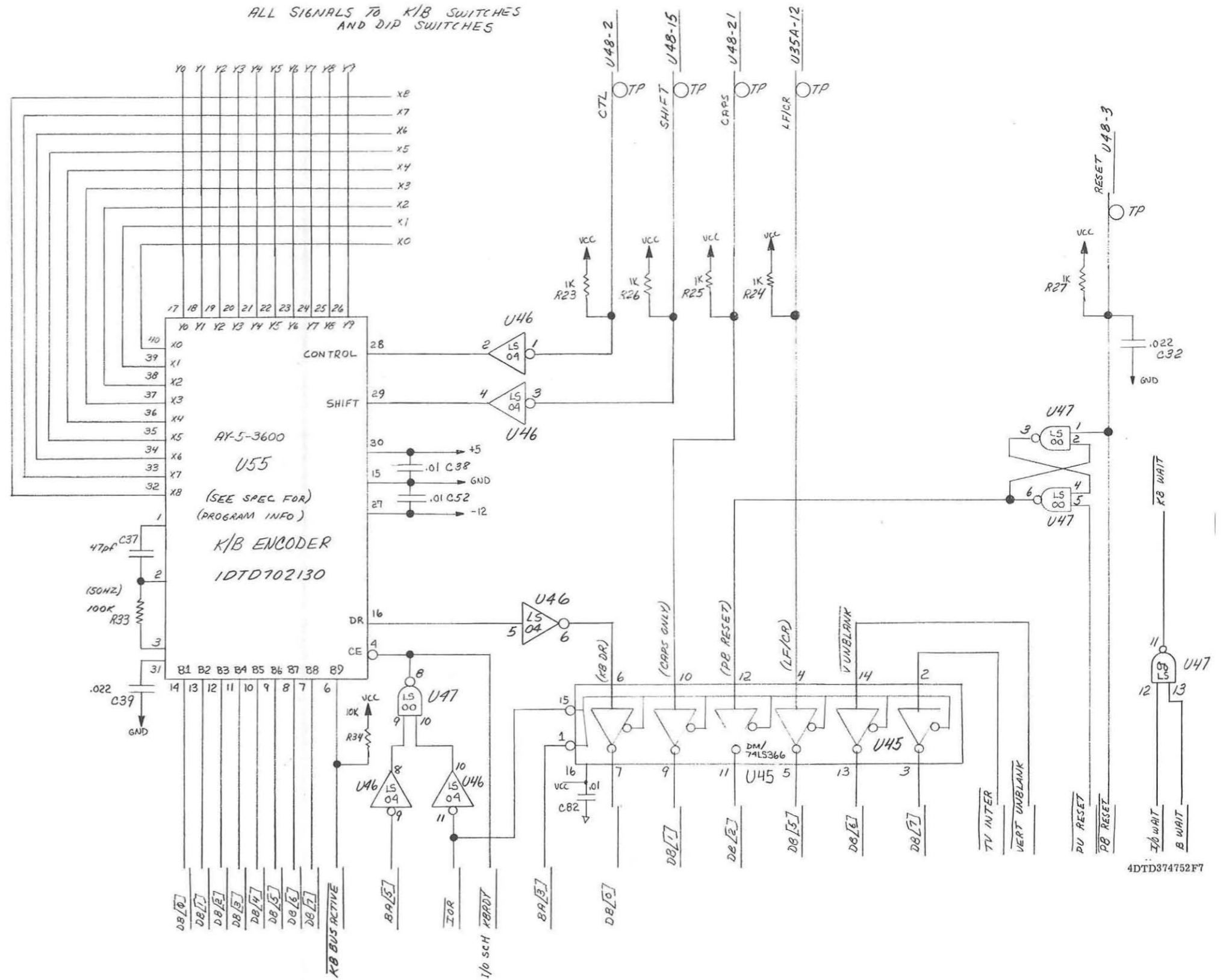


Figure B-5. Logic/Keyboard Assembly, Schematic Diagram (Sheet 7 of 9)

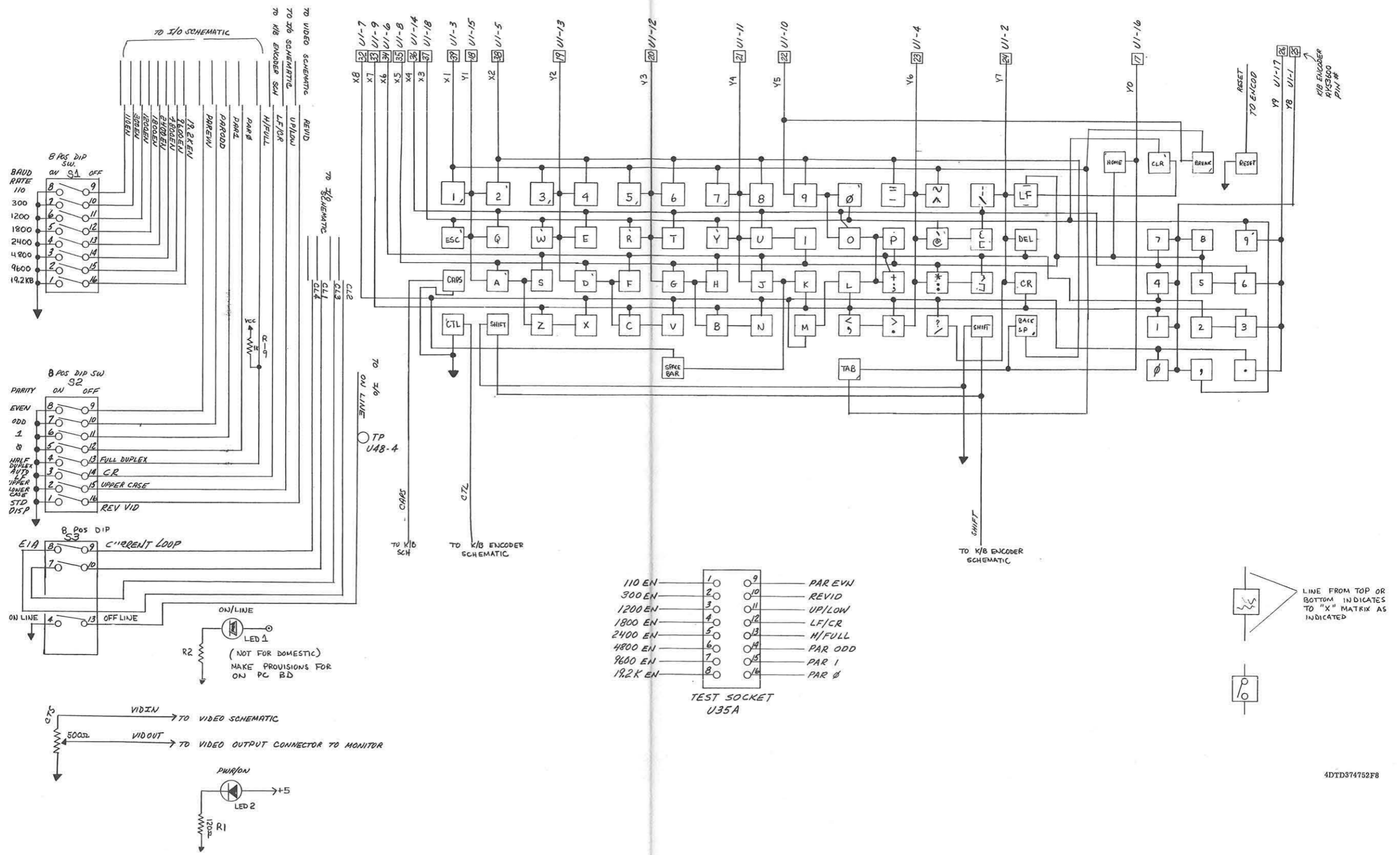
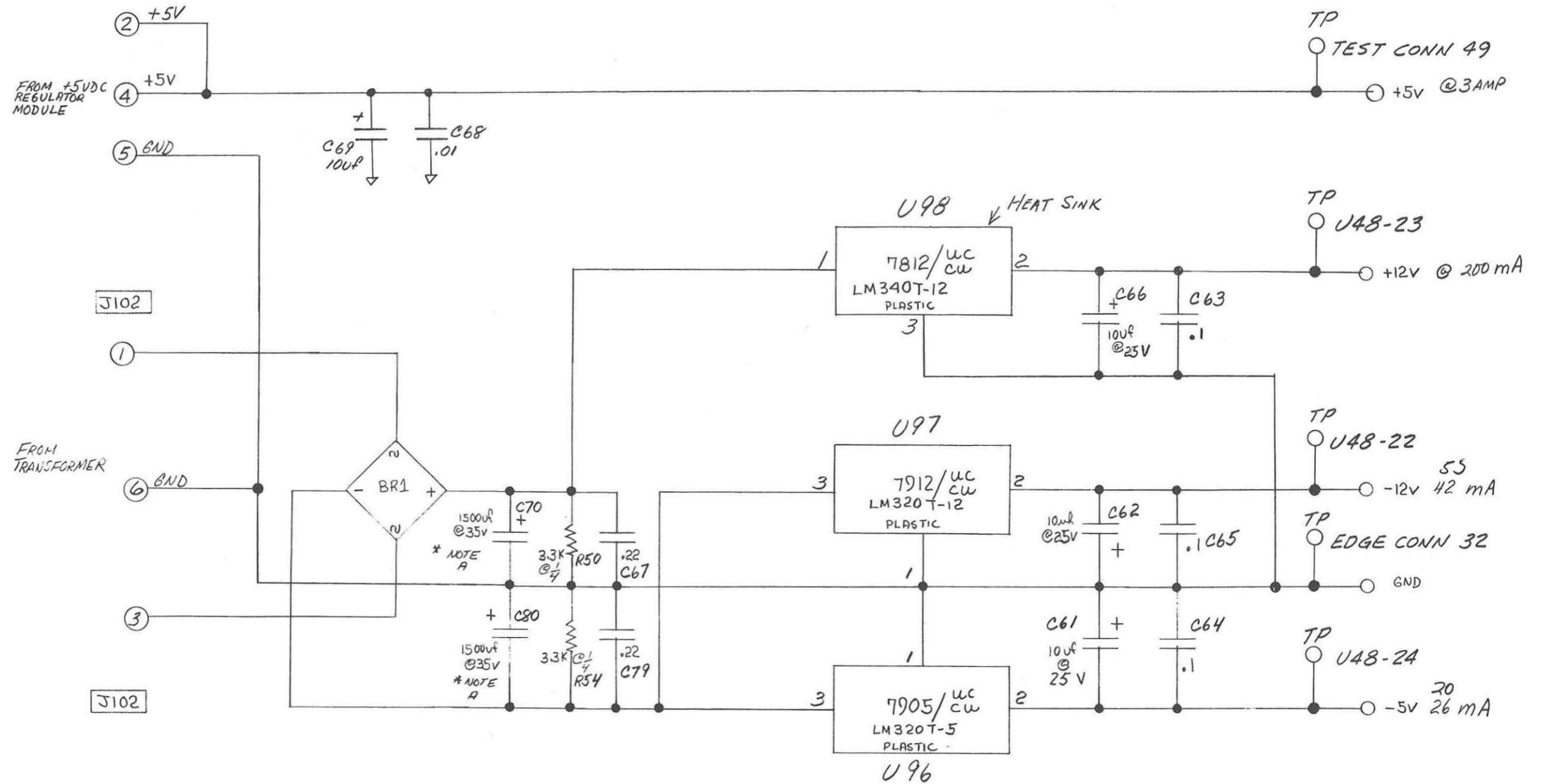


Figure B-5. Logic/Keyboard Assembly, Schematic Diagram (Sheet 8 of 9) B-14

4DTD374752F8



BR1 VARO VE18
 GI WLO2M
 EDAL B376-10

NOTE A: VALUE OF CAPACITOR MAY VARY DUE TO MANUFACTURER BETWEEN 1500µF → 2200µF

4DTD374752F9

Figure B-5. Logic/Keyboard Assembly, Schematic Diagram (Sheet 9 of 9) B-15

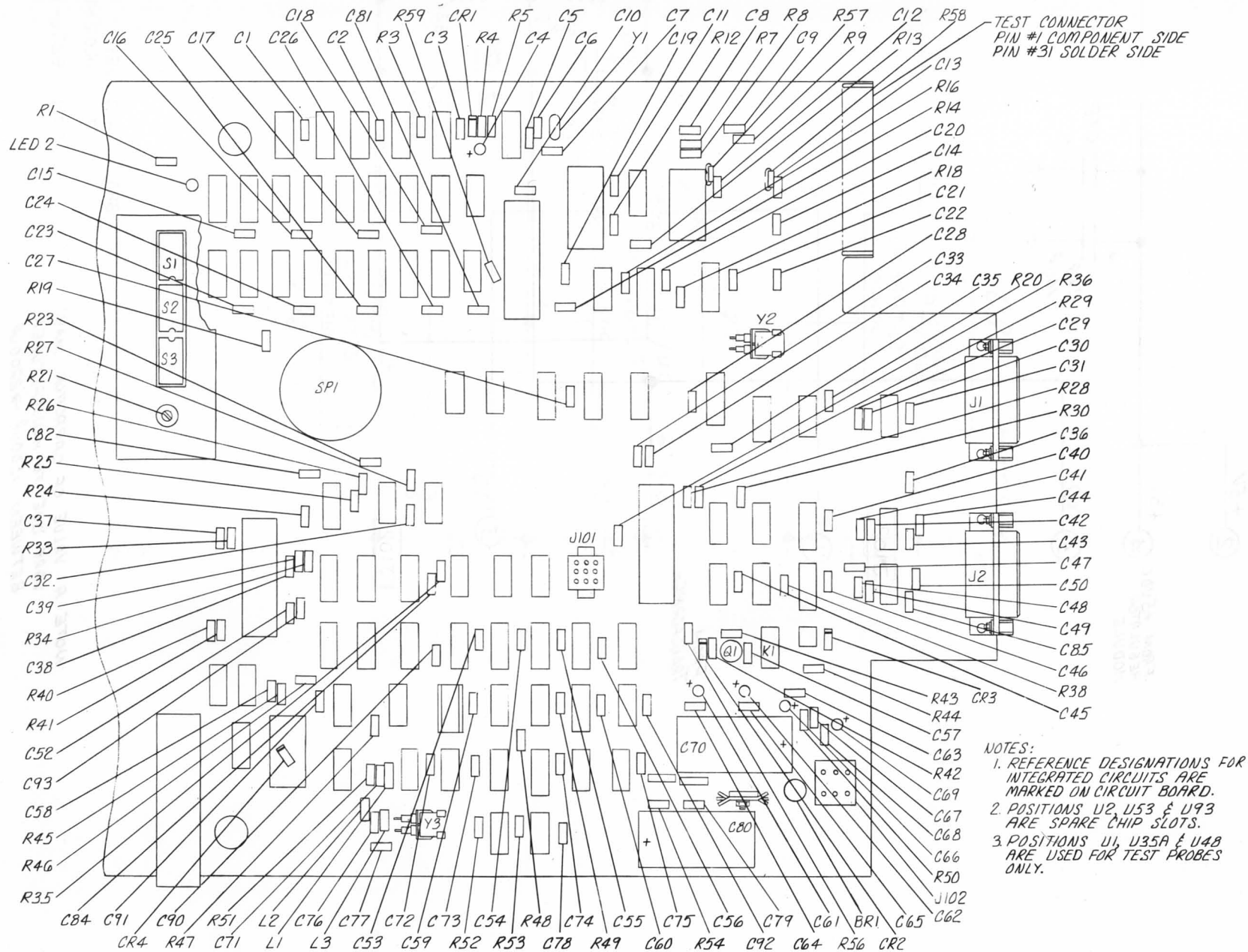
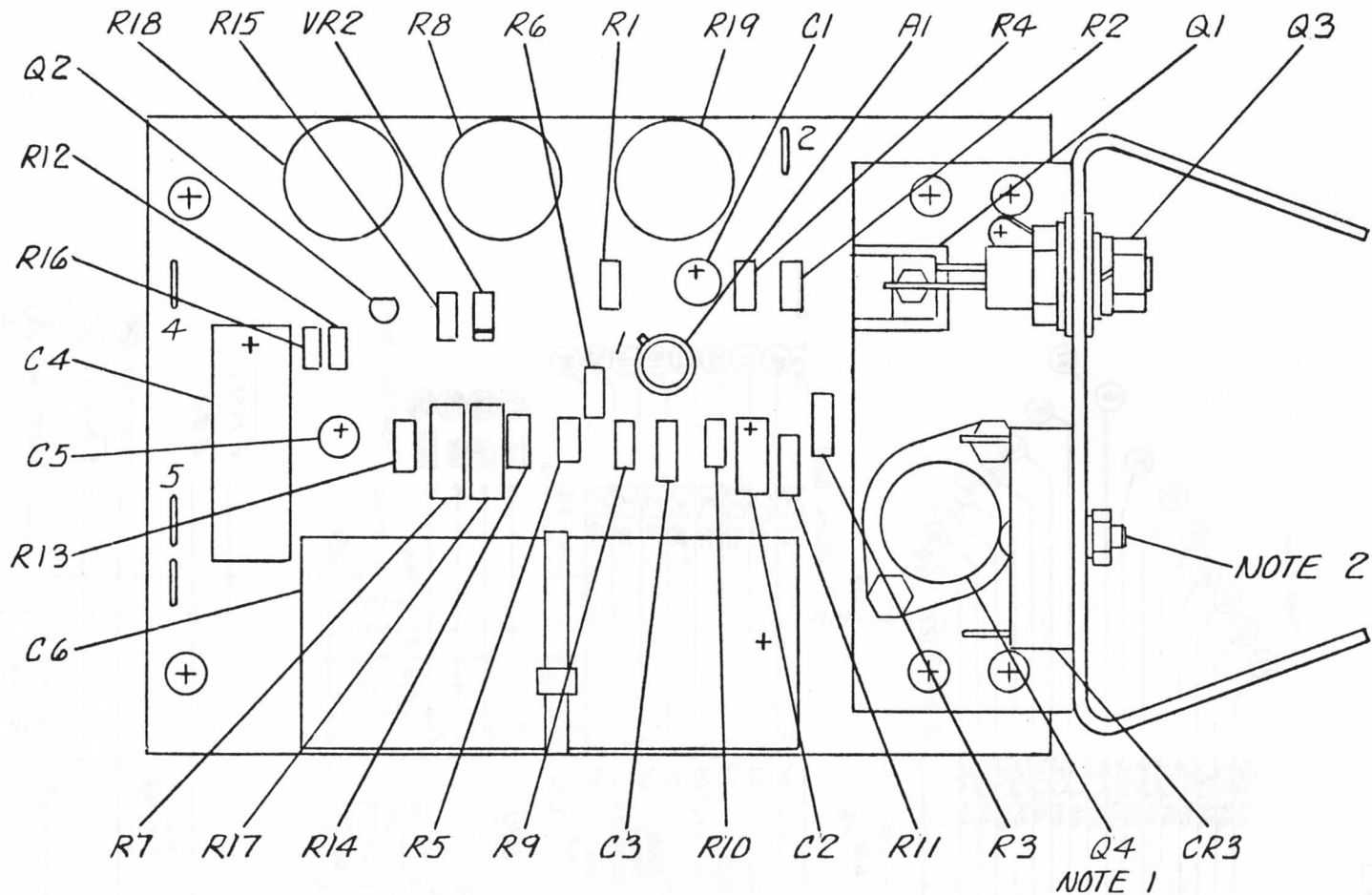


Figure B-6. Logic/Keyboard Assembly Part No. 4DTD155202, Parts Location



NOTES:

1. APPLY A THIN FILM OF THERMAL COMPOUND, HAZELTINE PART NO. 1DTD460003, TO MATING SURFACES OF Q4 AND HEAT SINK IF Q4 IS REPLACED.
2. TORQUE SCREW SECURING CR3 TO 10 ± 2 IN-LBS.

7707015

Figure B-7. Five-Volt Regulator, Parts Location

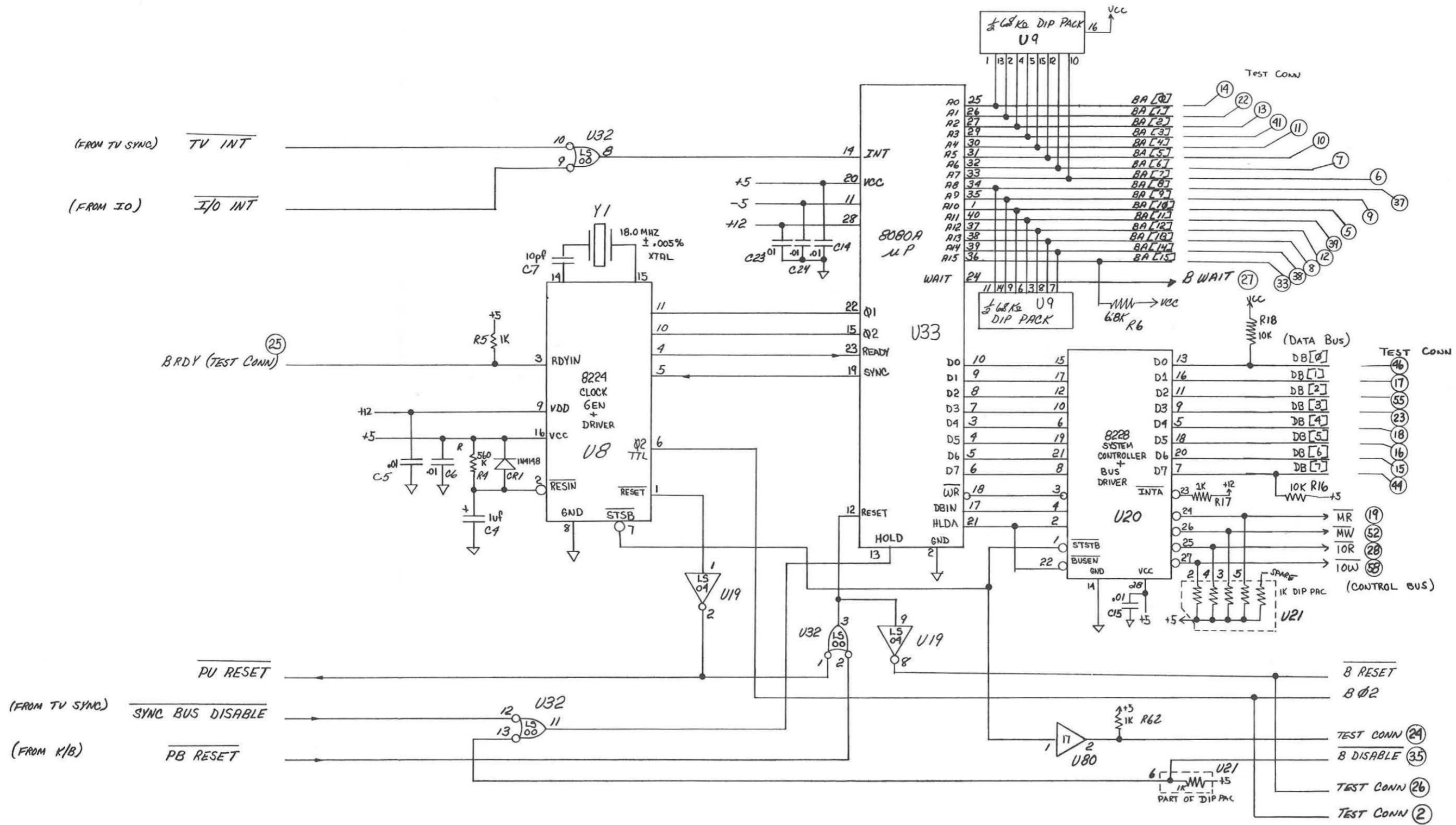
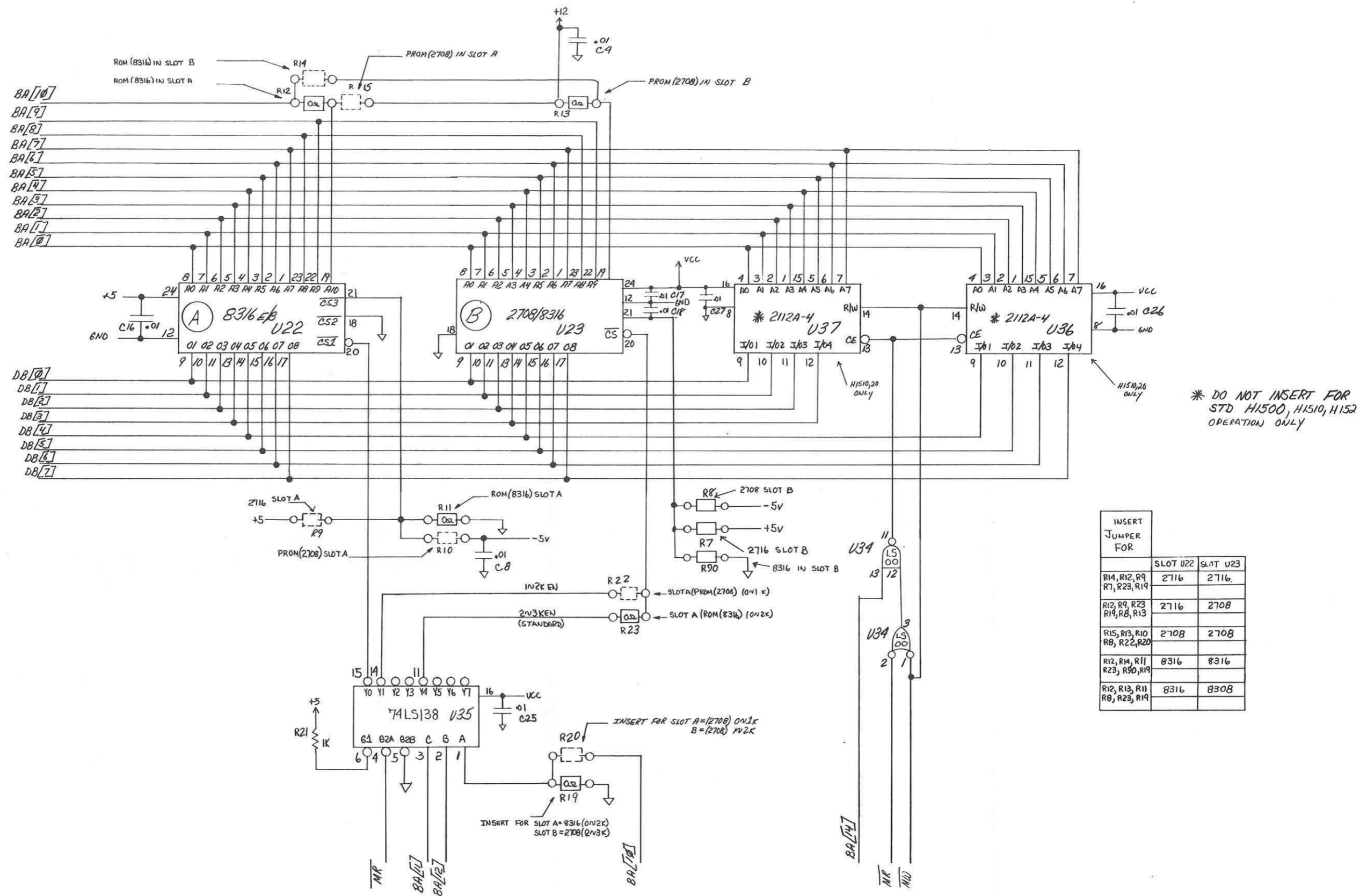


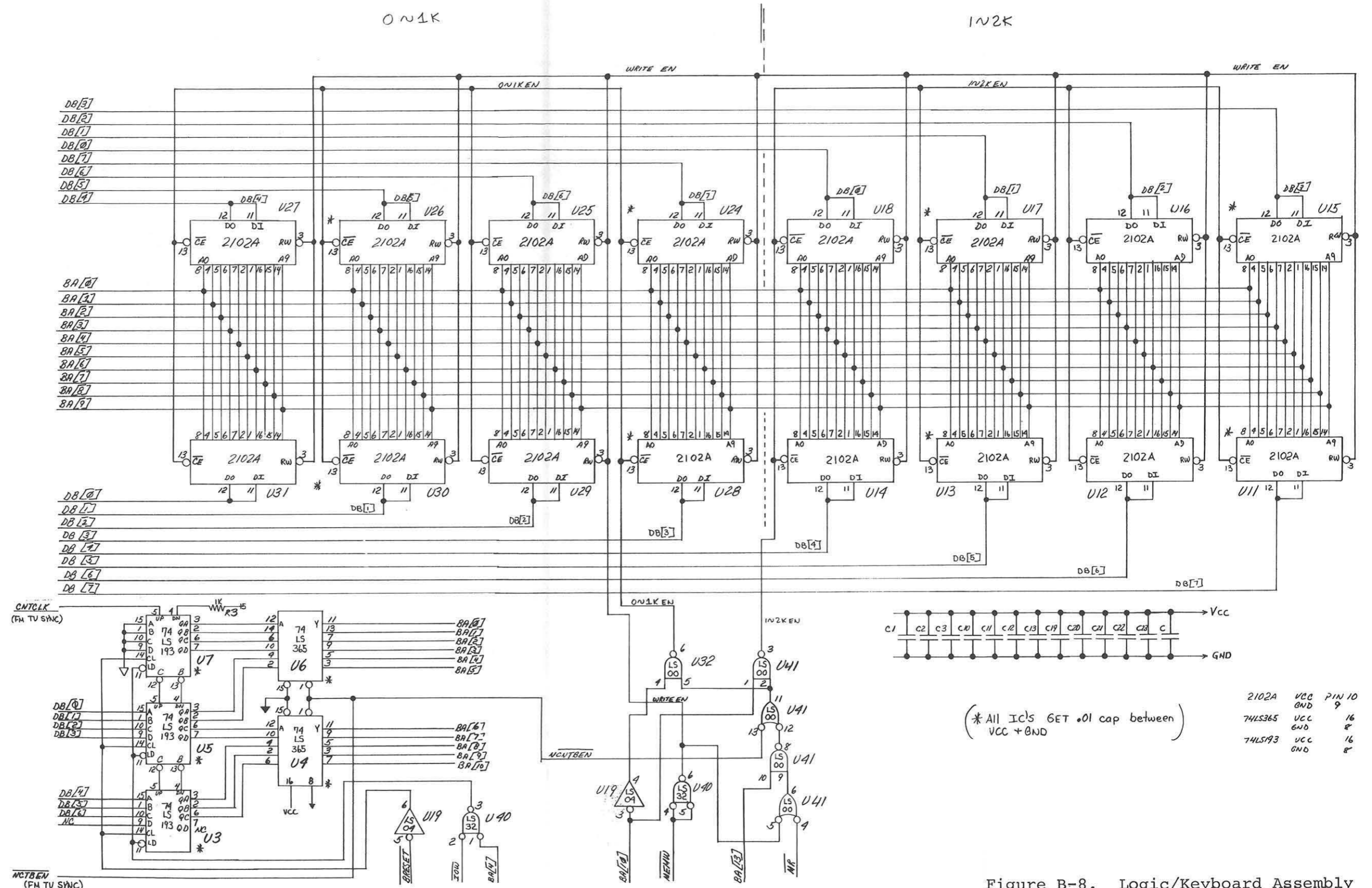
Figure B-8. Logic/Keyboard Assembly
 PN 4DTD155246-(), Schematic Diagram
 (Sheet 1 of 9)



* DO NOT INSERT FOR STD H1500, H1510, H152 OPERATION ONLY

INSERT JUMPER FOR	SLOT U22	SLOT U23
R14, R12, R9, R7, R23, R19	2716	2716
R13, R9, R23, R19, R8, R13	2716	2708
R15, R13, R10, R8, R22, R20	2708	2708
R12, R4, R11, R23, R9, R19	8316	8316
R12, R13, R11, R8, R23, R19	8316	8308

Figure B-8. Logic/Keyboard Assembly PN 4DTD155246-(), Schematic Diagram (Sheet 2 of 9)



(* All IC's GET .01 cap between VCC + GND)

IC	VCC	PIN 10
2102A	VCC	9
	GND	9
74LS365	VCC	16
	GND	8
74LS193	VCC	16
	GND	8

Figure B-8. Logic/Keyboard Assembly PN 4DTD155246-(), Schematic Diagram (Sheet 4 of 9)

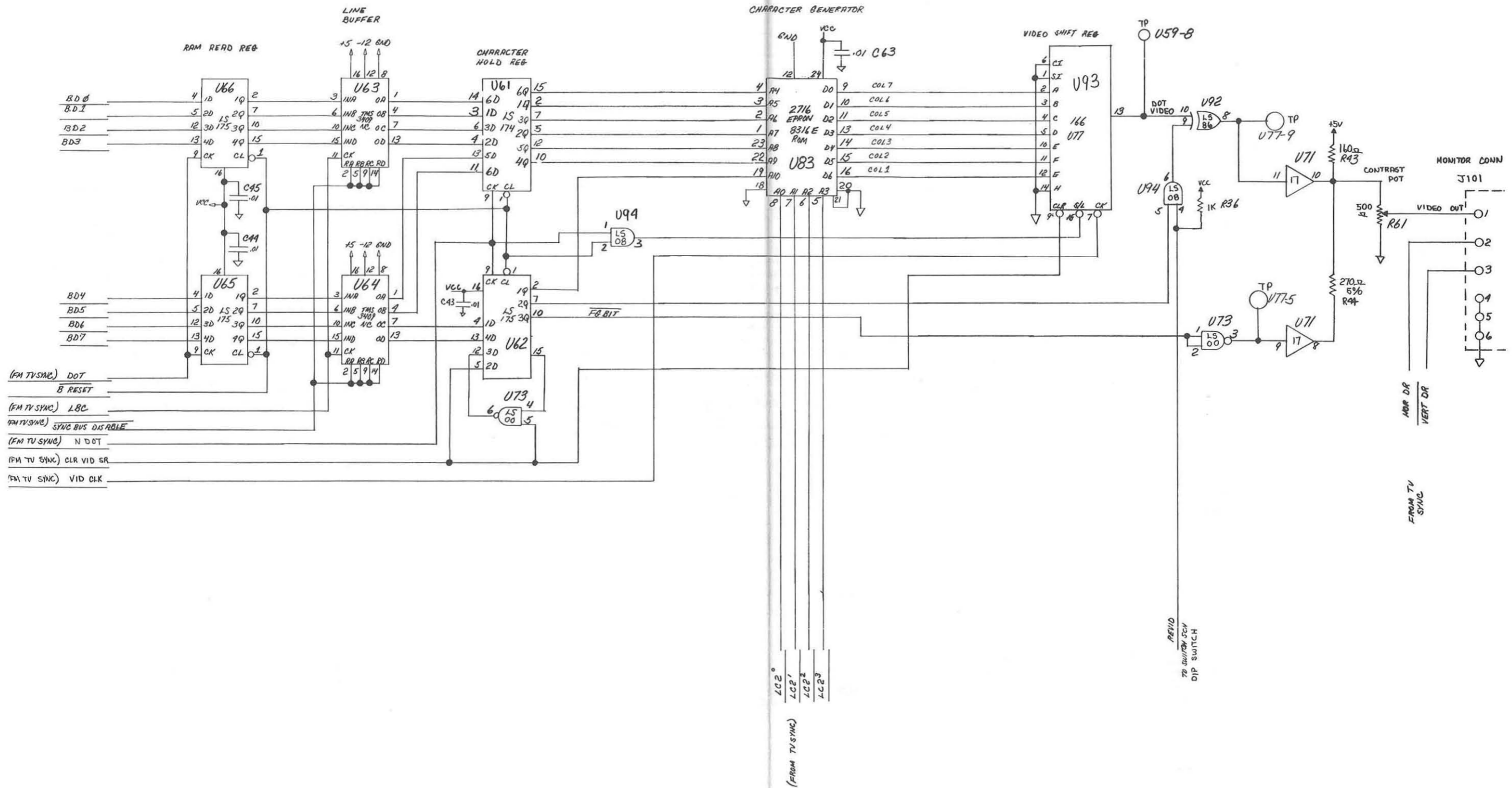


Figure B-8. Logic/Keyboard Assembly PN 4DTD155246-(), Schematic Diagram (Sheet 5 of 9)

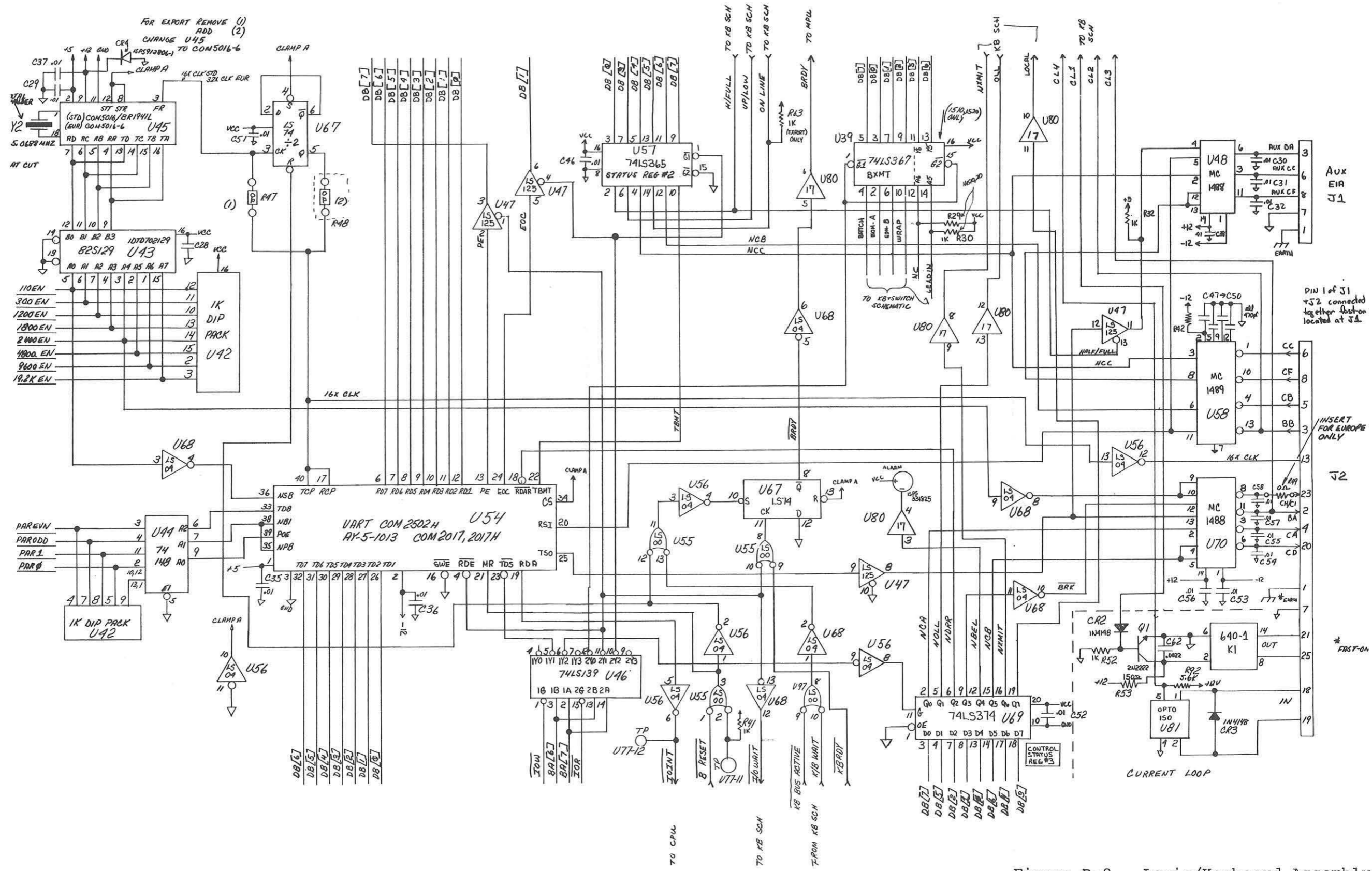


Figure B-8. Logic/Keyboard Assembly PN 4DTD155246-(), Schematic Diagram (Sheet 6 of 9)

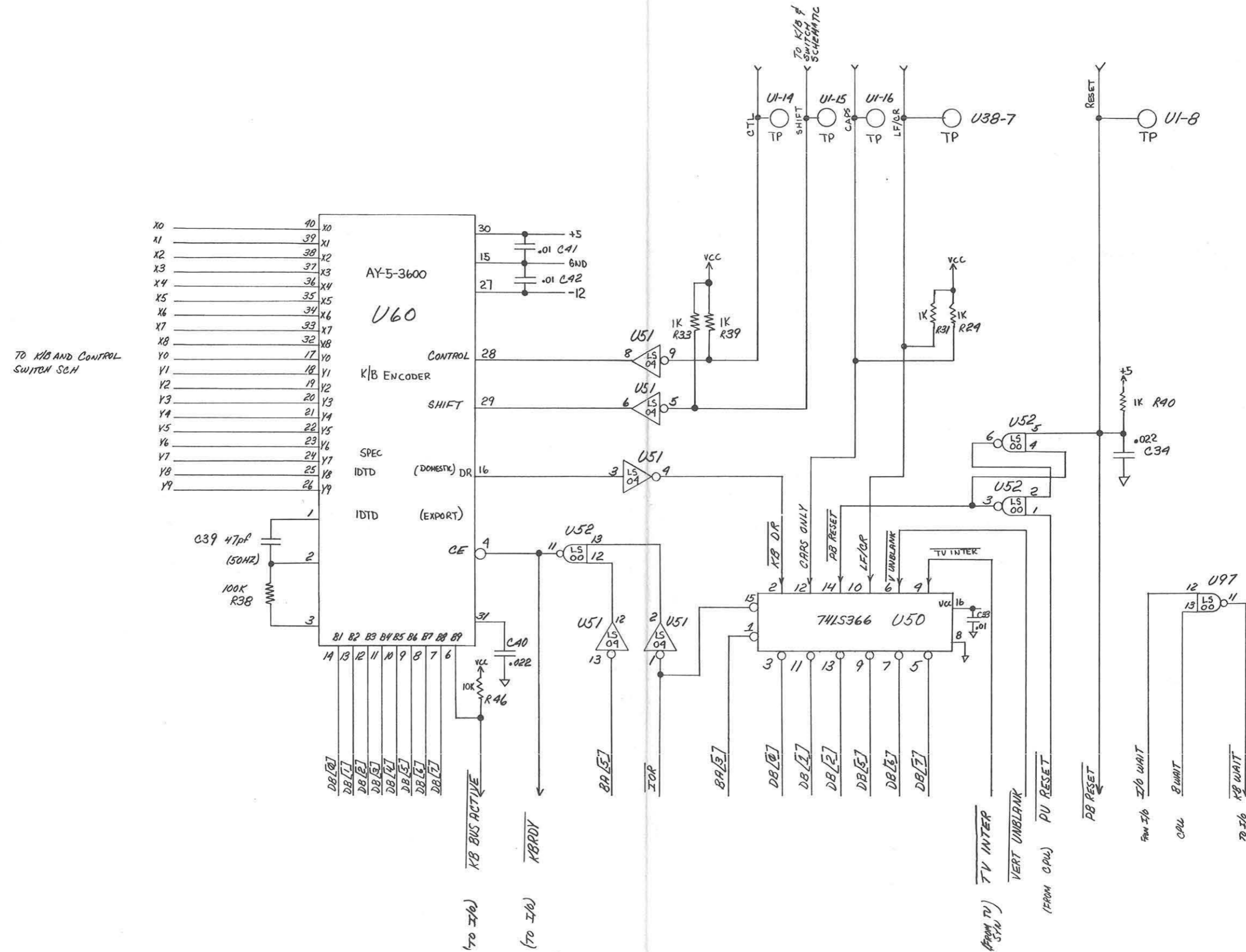


Figure B-8. Logic/Keyboard Assembly PN 4DTD155246-(), Schematic Diagram (Sheet 7 of 9)

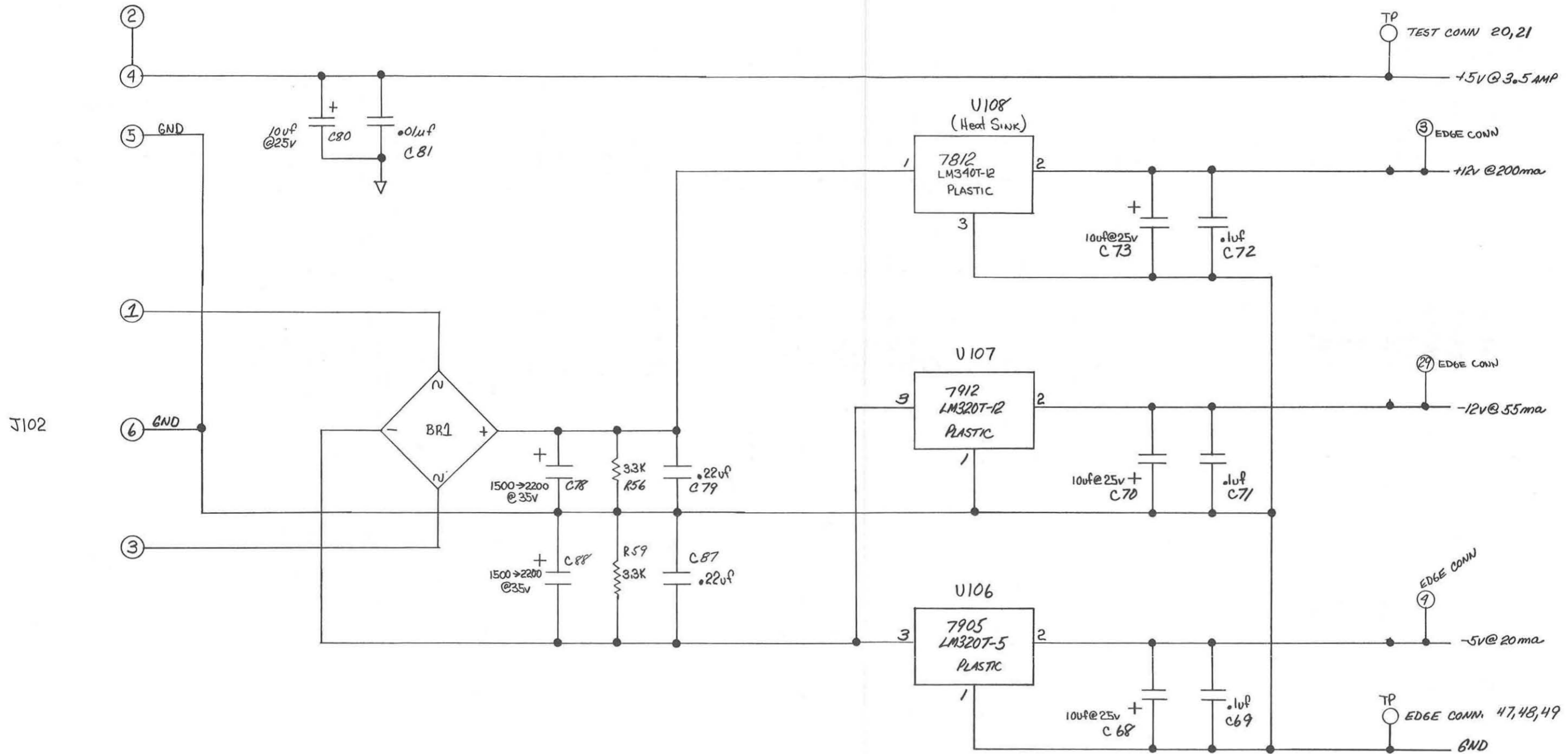


Figure B-8. Logic/Keyboard Assembly PN 4DTD155246-(), Schematic Diagram (Sheet 9 of 9)

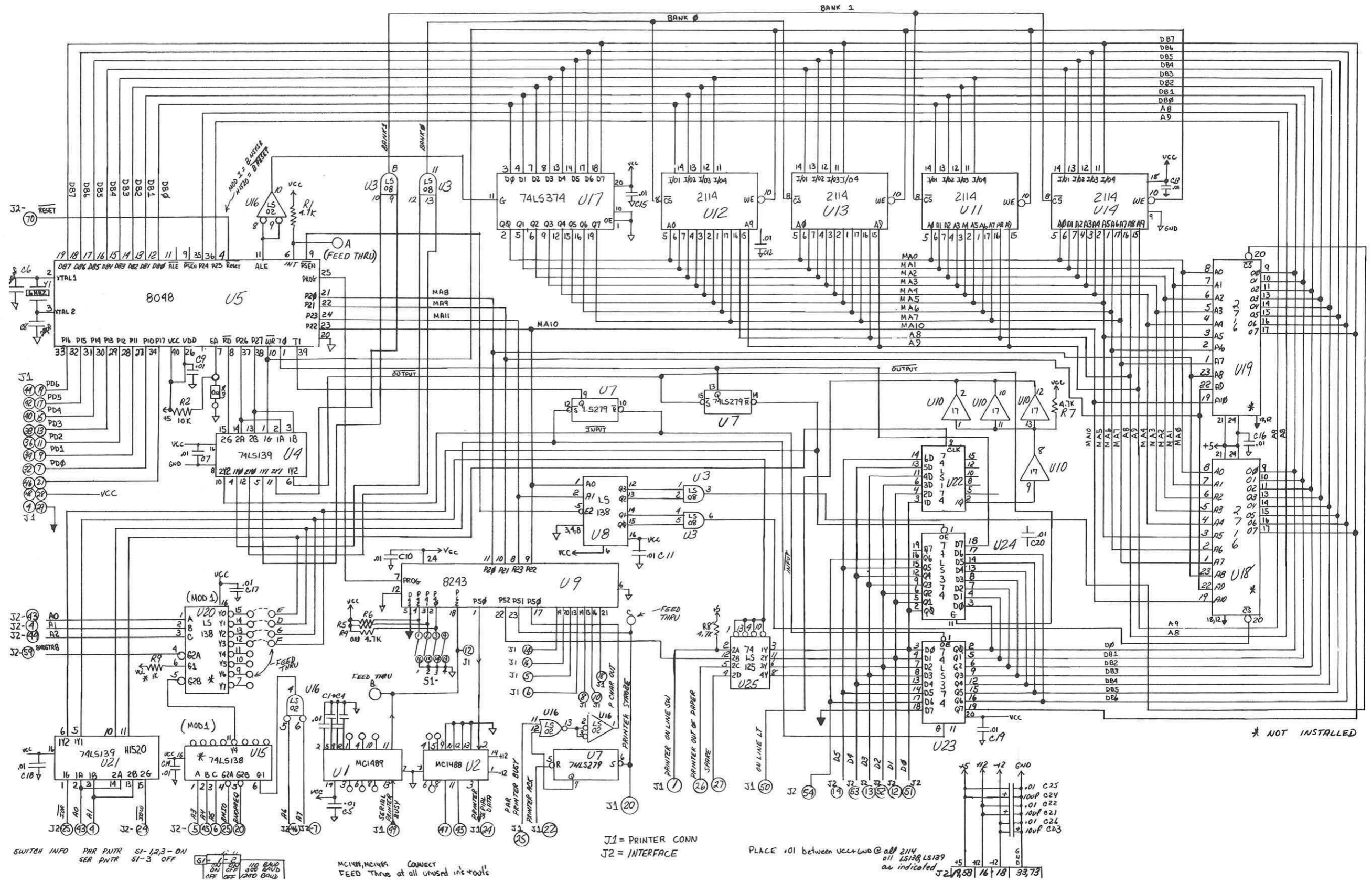


Figure B-9. Printer Buffer, Schematic

B-29/(B-30 blank)

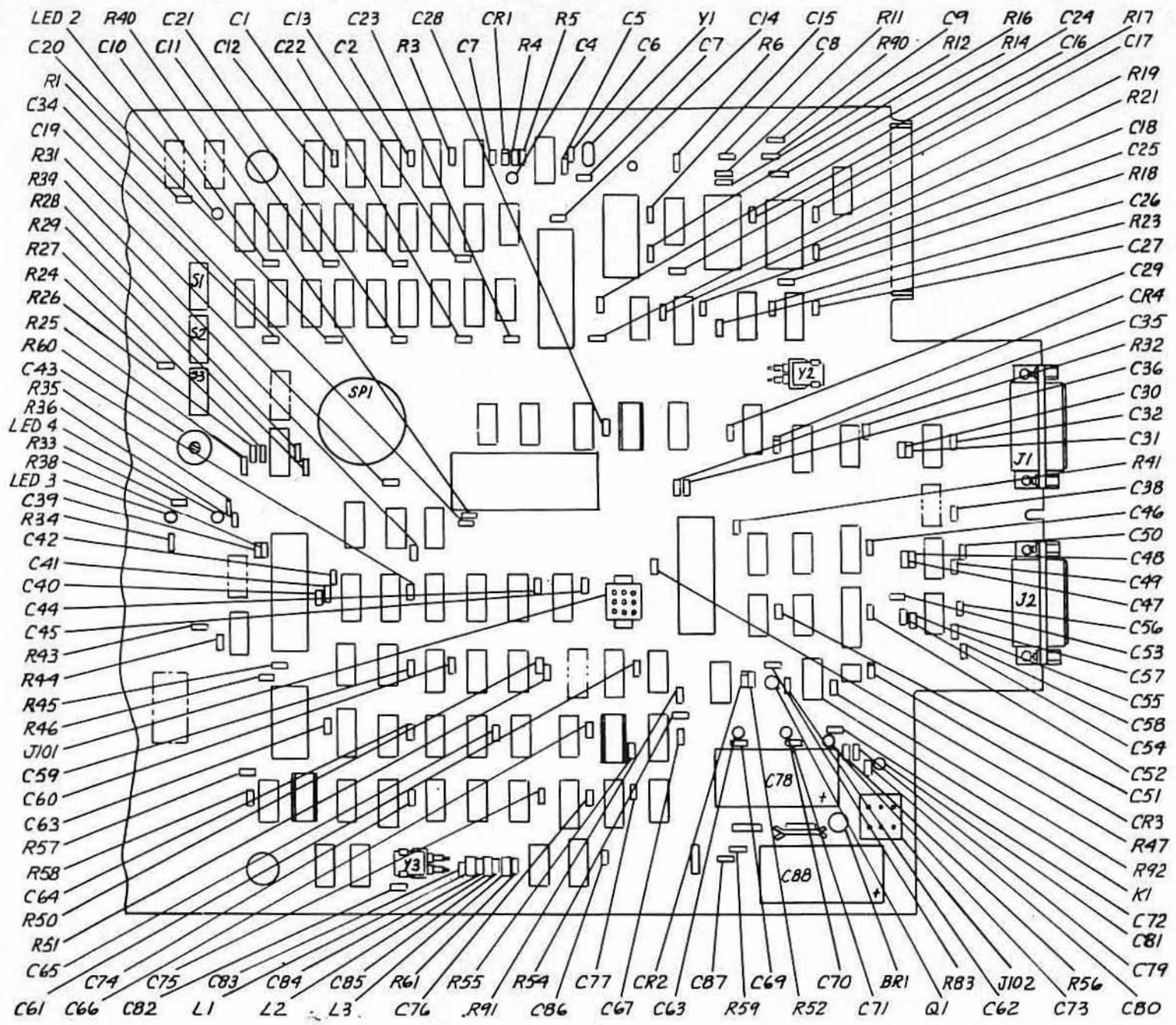


Figure B-11. Logic/Keyboard Assembly Part No. 4DTD155246-2, Parts Location

HI-1053A

APPENDIX C

EXPORT UNITS

C.1 In addition to the differences noted on the schematic diagrams for "export" versions, these units differ in the following areas:

Transmission Rates: 110, 200, 300, 600, 1200, 2400, 4800, or 9600 baud

Modes: No LOCAL mode

On-Line/Offline DIP switch and LED added (Model 1500), see figure C-1

On-Line/Offline key, On-Line LED and On-Line switch status LED added (Models 1510/20)

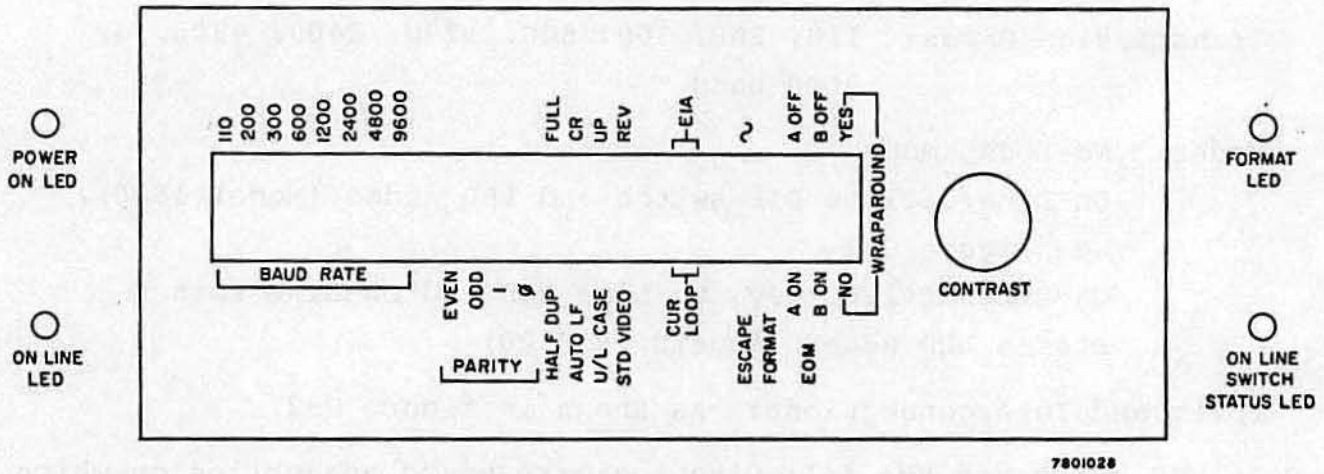
Power and Interconnections: As shown in figure C-2.

C.2 VDE units use the following logic/keyboard assemblies on which the I/O section of the logic/keyboard assembly, shown in figure C-3, has no current loop circuit:

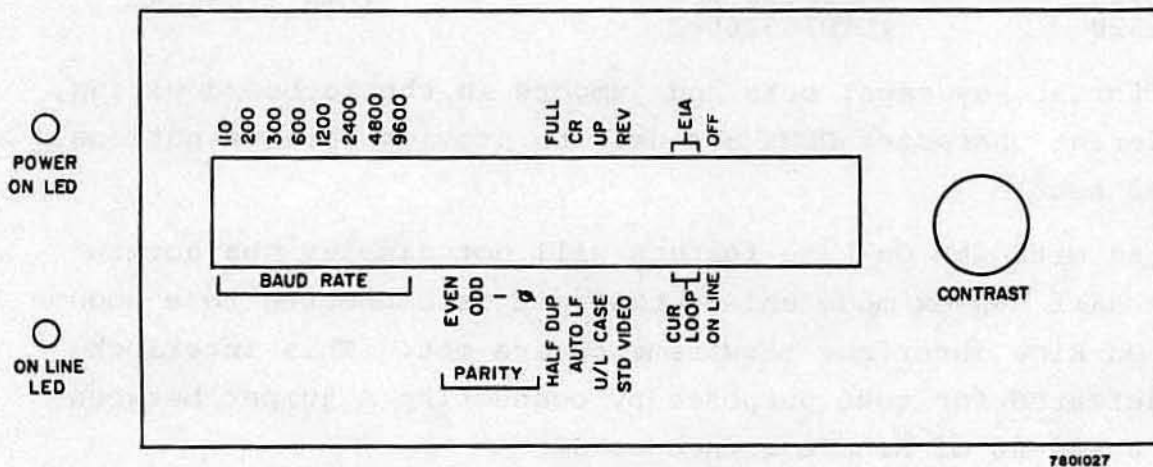
Model	Terminal Part No.	Logic/Keyboard Part No.
1500	4DTD155207-2	4DTD155278-1
1510	4DTD155255-2	4DTD155278-2
1520	4DTD155260-2	

C.3 Different key caps, cuts and jumpers in the keyboard wiring, and different character ROMs are used to provide various national character sets.

C.4 Units with the On-Line feature will not display characters keyed in half duplex mode unless the unit is connected to a modem and the On-Line interface requirements are met. This interlock can be defeated for test purposes by connecting a jumper between pins 5, 6 and 20 of EIA/CL connector J2.



a) Models 1510 and 1520



b) Model 1500

Figure C-1. Controls and Indicators Under Access Panel, Export Units

TABLE A

JUMPER INFORMATION TO SELECT DESIRED MAINS INPUT TO TRANSFORMER T1		
JUMPER	AC VOLTAGE RANGE	FUSE F1
2-5	115V ±10% VRMS	TYPE 3AG SLO BLO 1 1/4 AMP
3-6		
5-7		
3-5	220V ±10% VRMS	TYPE 3AG SLO-BLO 3/4 AMP
2-7		
3-4	240 ±10% VRMS	
1-7		

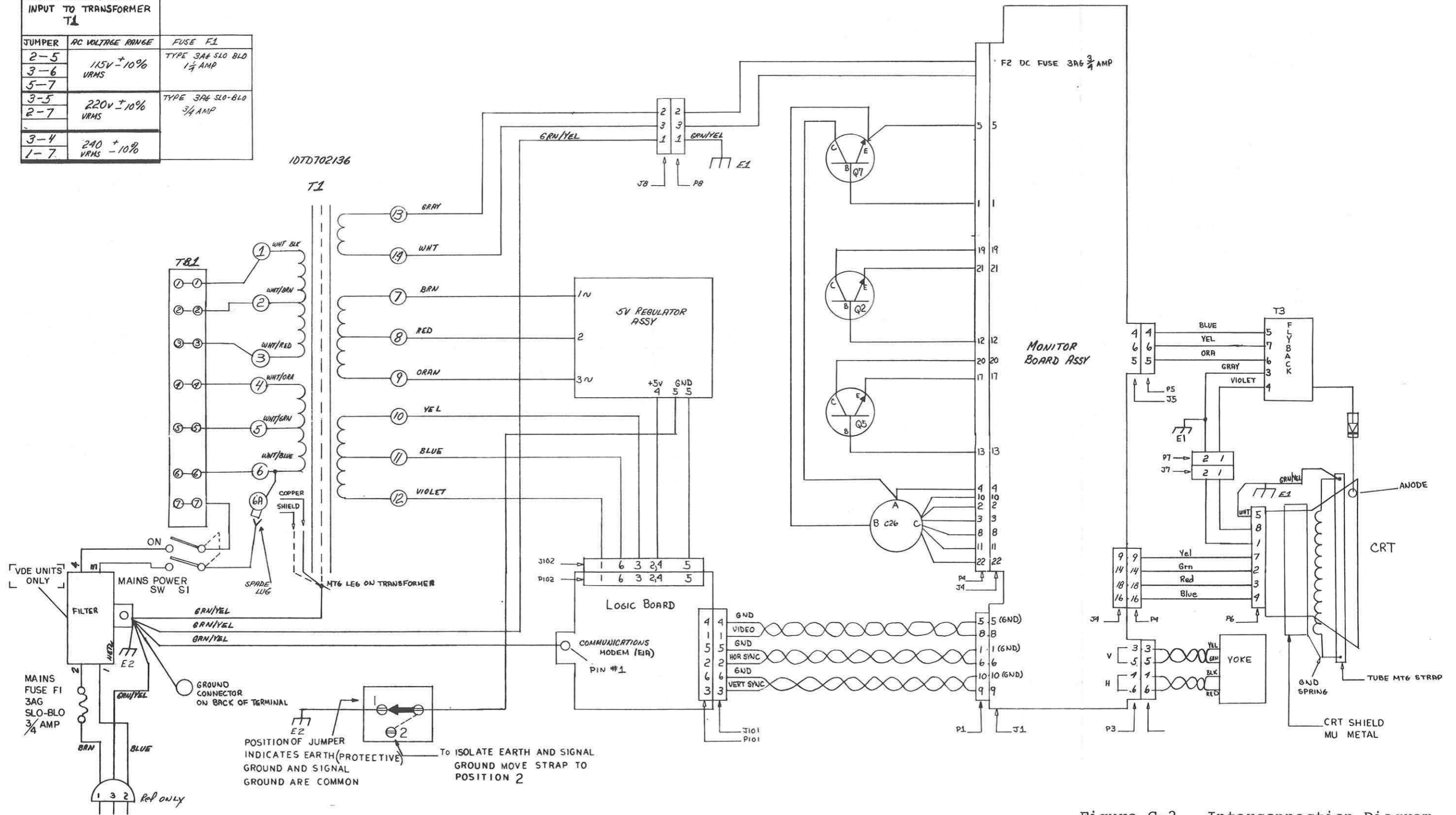


Figure C-2. Interconnection Diagram, Dwg 4DTD964406

C.5 Where a terminal does not have a character used as a cursor address or remote command, that character which generates the same code must be substituted as listed in the accompanying table.

U.S.	Denmark	England	France	Germany	Italy	Spain	Sweden
#		æ			æ		
@			à	ö	ö		
[Æ		o	Ä	o		Ä
\	ø		é	Ö	é	Ñ	Ö
]	Å		ö	Ü	é		Å
{	æ		é	ä	ä		ä
:	o		ù	ö	ö	Ñ	ö
}	å		è	ü	è		å
^	o						Ü
\$							ÿ

APPENDIX D

SUMMARY OF REMOTE COMMANDS
(ALL MODELS)

REMOTE COMMANDS	LEAD-IN* REQD (X)	KEY STROKE	ASCII CODE	DECIMAL
Home Cursor	X	Control-R	DC2	18
Up Cursor	X	Shift-Line Feed	FF	12
Down Cursor	X	Control-K	VT	11
Left Cursor		Back Space	BS	8
Right Cursor		Shift-Backspace	DLE	16
Address Cursor	X	Control-Q	DC1,X,Y	17,X,Y
Read Cursor Address	X	Control-E	ENQ	5
Clear Screen	X	Control/Shift-L	FS	28
Clear Foreground	X	Control/Shift-M	GS	29
Clear to End-of-Line	X	Control-O	SI	15
Clear to End-of-Screen	X	Control-X	CAN	24
Clear to End-of-Screen - background spaces	X	Control-W	ETB	23
Background Follows	X	Control-Y	EM	25
Foreground Follows	X	Control/Shift-O	US	31
Delete Line	X	Control-S	DC3	19
Insert Line	X	Control-Z	SUB	26
Keyboard Lock	X	Control-U	NAK	21
Keyboard Unlock	X	Control-F	ACK	6
Audible Alarm		Control-G	BEL	7
Tab		Tab	HT	9

*Lead-in Code = ASCII ~, Decimal 126

SUMMARY OF REMOTE COMMANDS
1510/1520 ONLY

REMOTE COMMANDS	LEAD-IN* REQD (X)	KEY STROKE	ASCII CODE	DECIMAL
Set Format Mode	X	#	#	35
Return to Switches** (Format, Half, Full)	X	\$	\$	36
Batch Transmit**	X	%	%	37
Line Transmit	X	.	. (period)	46
Page Transmit	X	((40
Unprotected**	X	,	, (comma)	44
Protected and Unprotected	X	+	+	43
Back Tab	X	C _T	DC4	20
Send Status	X	-	-	45
Remote Xmit	X	C _N	SO	14
Non Stored Return	X	Return	CR	13
Remote Print				
1520 ONLY				
Remote Print	X	CS _N	RS	30
On-line Print-Display	X	/	/	47
On-line Print-No Display	X	*	*	42
Printer Off Line**	X	?	?	63

* Lead-in Code = ASCII ~, column 7, row 14 - DECIMAL 126
or = ASCII ESC, column 1, row 14 - DECIMAL 27

**Default condition at turn on or after reset