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MEGABITS TO MEGABYTES: Bubble Memory System Design and Board Layout

STEVEN KNAPP
APPLICATIONS ENGINEER
INTEL CORPORATION

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MEGABITS TO MEGABYTES
Bubble Memory System Design and Board Layout

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INTRODUCTION

There are many advantages in designing with Intel bubble memory components. The sophisticated seven-component bubble memory system represents the most integrated solution to reliable, non-volatile memory design. In addition, the VLSI Bubble Memory Controller (BMC) makes interfacing to any microprocessor easy.

Furthermore, there are no form factor limitations when designing with Intel bubble memory. The integrated solution allows the designer to lay out his boards to his specifications. However, there are a few unique considerations to be aware of before designing any bubble memory system.

It is the purpose of this applications note to inform the reader of the special considerations involved in designing a reliable bubble memory system. The attention paid to a few, simple design guidelines will insure the success of a bubble memory.

In addition, this application note will make use of illustrative examples taken from proven, reliable Intel bubble memory board products (namely the BPK-72A Bubble Prototype Kit and the iSBX-251 board). Though both Intel board products are single-bubble systems, the employed design techniques are helpful even for multiple-bubble systems. Each example will take a step-by-step approach to make board layout even easier for a bubble memory user who is designing his own custom board.

Since this application note would typically be read by those about to design their own custom bubble memory board, it is assumed that the reader has some previous familiarity with bubble memory system basics (i.e., from the BPK-72A Prototype Kit, or from other application notes).

SYSTEM OVERVIEW

The Intel bubble memory solution consists of a highly sophisticated Bubble Memory Controller (BMC) which can individually support up to an entire megabyte or eight Bubble Storage Units (BSUs).

7220 Bubble Memory Controller (BMC)

The 7220 is a 40-pin VLSI chip (0.6″ center) which generates the timing and control signals necessary for proper operation of the remaining support circuitry in each BSU. The 7220 also provides a versatile and convenient microprocessor interface.

Each Bubble Storage Unit (BSU) contains the following six components:

7110A Magnetic Bubble Memory (MBM)

The 7110A is a high-density, highly reliable, one-megabit, non-volatile solid state memory based on magnetic bubble technology. It is contained in a 20-pin leaded package (0.75″ center) surrounded by a mu-metal magnetic shield.

7230 Current Pulse Generator (CPG)

The 7230 is a 22-pin chip (0.4″ center) based on bipolar technology. The 7230 generates the necessary waveforms to input and output data from the 7110.

7242 Formatter Sense Amplifier (FSA)

The 7242 is a dual formatter/sense amplifier which interfaces directly with the 7110A MBM. It is responsible for detecting and enabling the generation of magnetic bubbles within the 7110A. The 7242 also performs the additional tasks of data formatting, error correcting, and mapping the redundancy built into the 7110A. The 7242 is a 20-pin chip with a 0.3″ center.

7250 Coil Predriver (CPD)

The 7250 works in conjunction with the two 7245 Drive Transistors to supply the rotating magnetic field that moves the magnetic bubbles inside the 7110A. It has 16 pins and rests on a 0.3″ center.

7254 Drive Transistors

The 7254 is a quad VMOS transistor package. Each 7254 works in conjunction with the 7250 to provide the rotating magnetic field. Two 7254s are required in each BSU. Additionally, each 7254 has 14 pins and also rests on a 0.3″ center.

SYSTEM EXPANSION

The Intel bubble memory component solution represents the easiest method to implement a highly reliable memory ranging from one megabit to one megabyte in size. Each sophisticated 7220 Bubble Memory Controller can control up to eight Bubble Storage Units (BSUs) at 0°C to 75°C and four BSUs at −20°C to +85°C. Each BSU is capable of storing 128 kbytes of information. Figure 1 shows a block diagram of an expanded bubble memory system.

Although a system may contain any number of BSUs up to eight per 7220 controller, typically the BSUs are grouped in powers of two (i.e.–two, four, or eight) to take advantage of the special parallel operation capabilities built into the Intel bubble memory support circuitry. However, any number of BSUs up to eight can be operated serially. System expansion requires no additional TTL parts when there are eight or less BSUs on a card.

This application note, therefore, will only address systems containing from one to eight BSUs and a single BMC on a card. Expanding a bubble memory system is then as easy as bussing the appropriate timing and control signals. A schematic for a complete four-bubble (512 kbytes) system is shown in Figure 2.

In a standard design, one controller and one BSU will occupy approximately 16 square inches of board real estate. Each additional BSU added to the system (MBM and support circuitry only, no controller) will occupy only 9 more square inches. For example, a four-bubble system will occupy 16 square inches for the first BSU and controller, plus 27 more square inches for the three remaining BSUs (3 x 9 sq. in.) for a total of 43 square inches for the entire system. Using these board real estate guidelines, a four-bubble system is easily accommodated on a Multibus, Eurocard, or VME board. Larger systems (i.e., more than four bubbles) require a much larger, bulkier, and typically non-standard circuit board. Therefore, it is suggested that the designer only place four BSUs and controller on any given board.

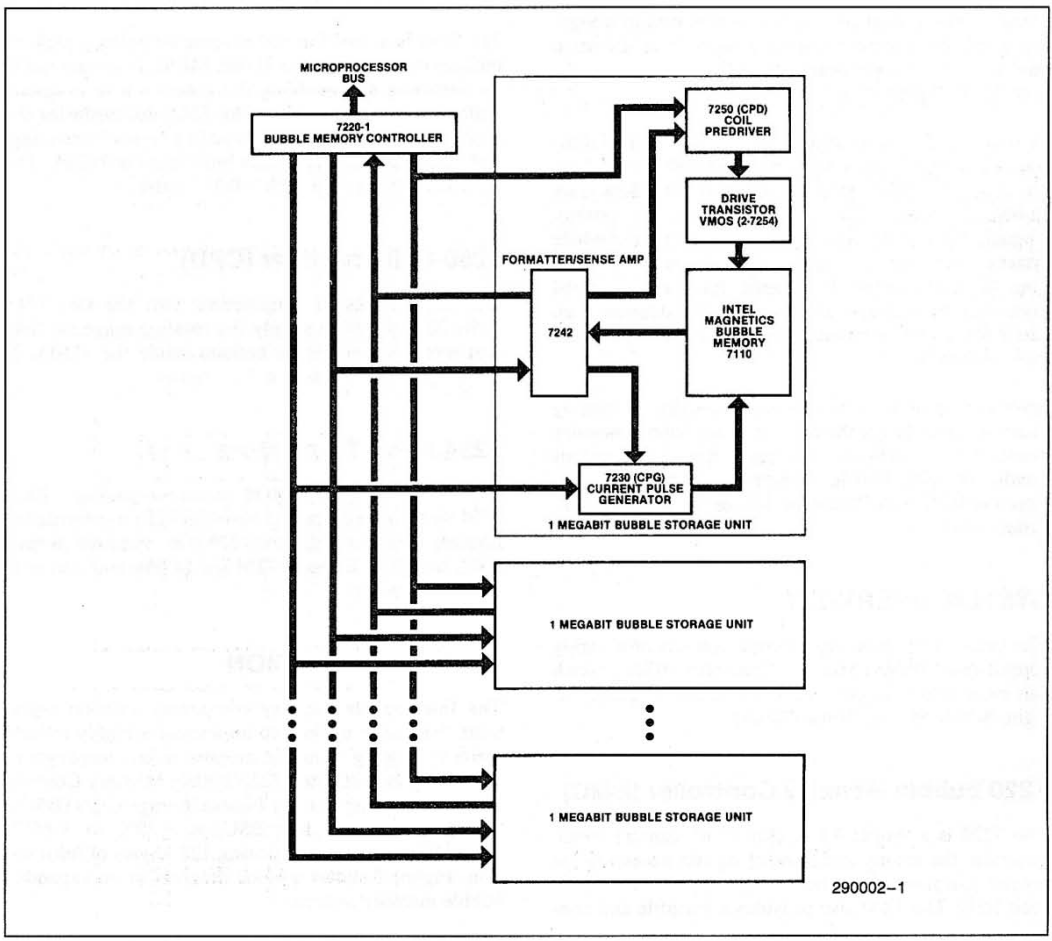

Figure 1. A Block Diagram of a Multiple Bubble Memory System

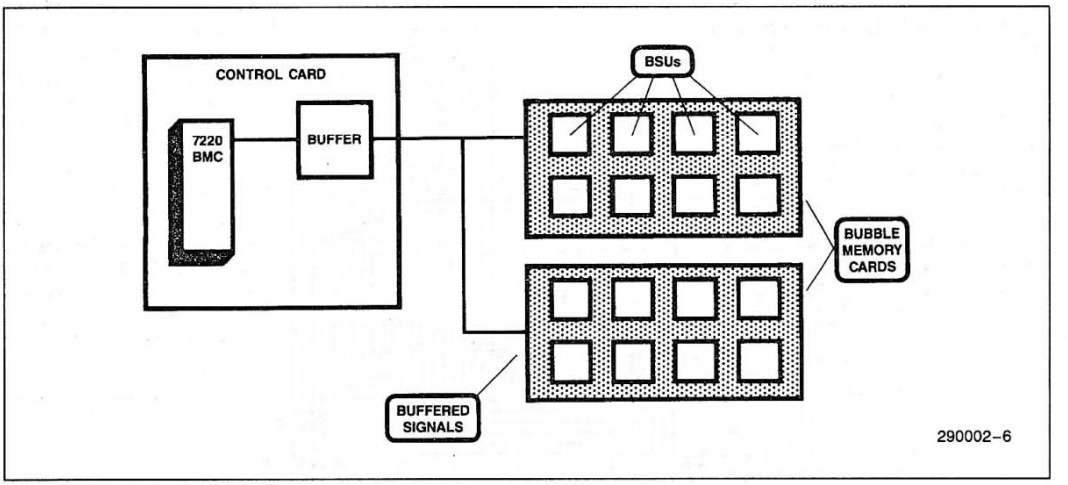

Figure 3. Bubble Memory Designed with Multiple Bubble Memory Cards and a Single Controller

Though it is possible to expand a bubble memory beyond one megabyte level by using multiple banks of BSUs (eight to a bank) and a single controller as shown in Figure 3, this is not the recommended method since there is a much easier, less expensive, and more reliable method. In order to switch between various banks of bubble memory, additional logic must be added to buffer the necessary timing and control lines from the single controller. A more reliable and economical solution is to build multiple cards each containing its own dedicated controller and four to eight BSUs.

With the dedicated controller solution as shown in Figure 4, a great deal of time, cost, and effort is saved. The design and cost of the complicated buffering circuit to

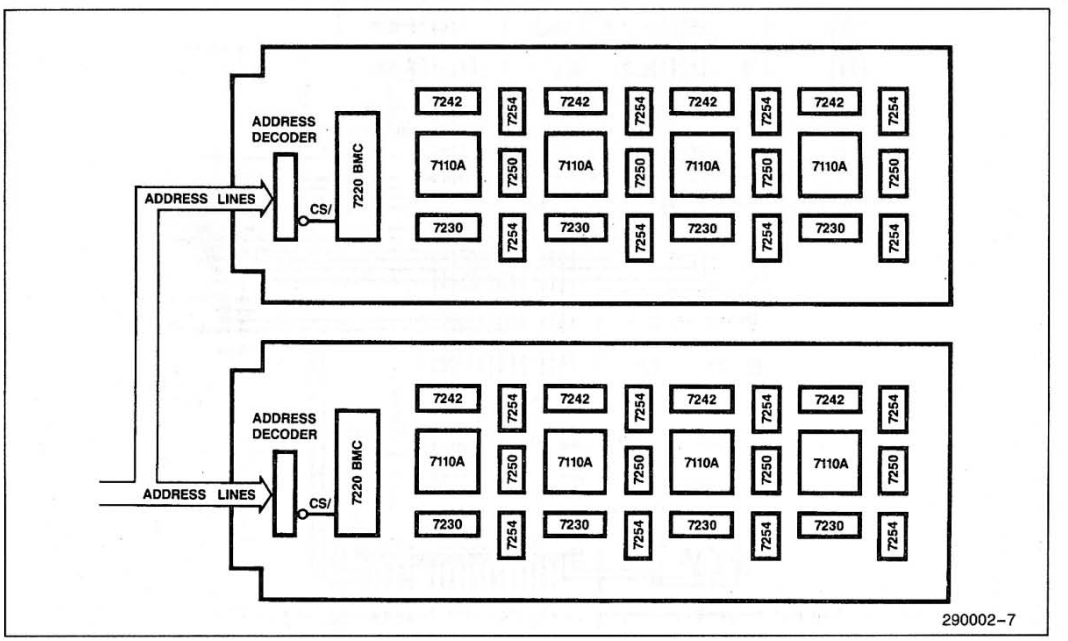

Figure 4. Bubble Memory Designed Using a Dedicated Controller per Bubble Memory Circuit Board

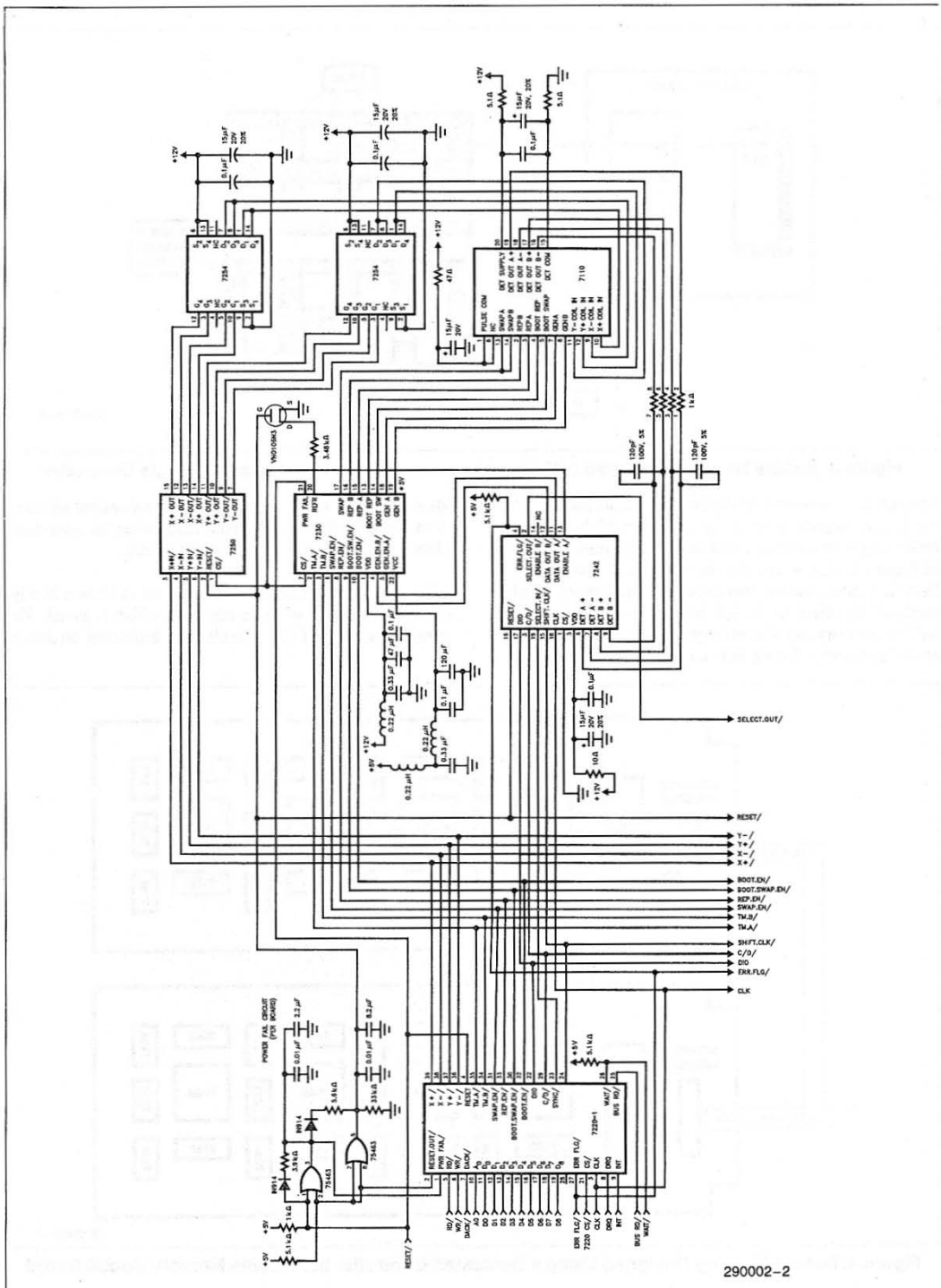

Figure 2a. A Complete Schematic of a Four-Bubble (512 kbyte) Bubble Memory System

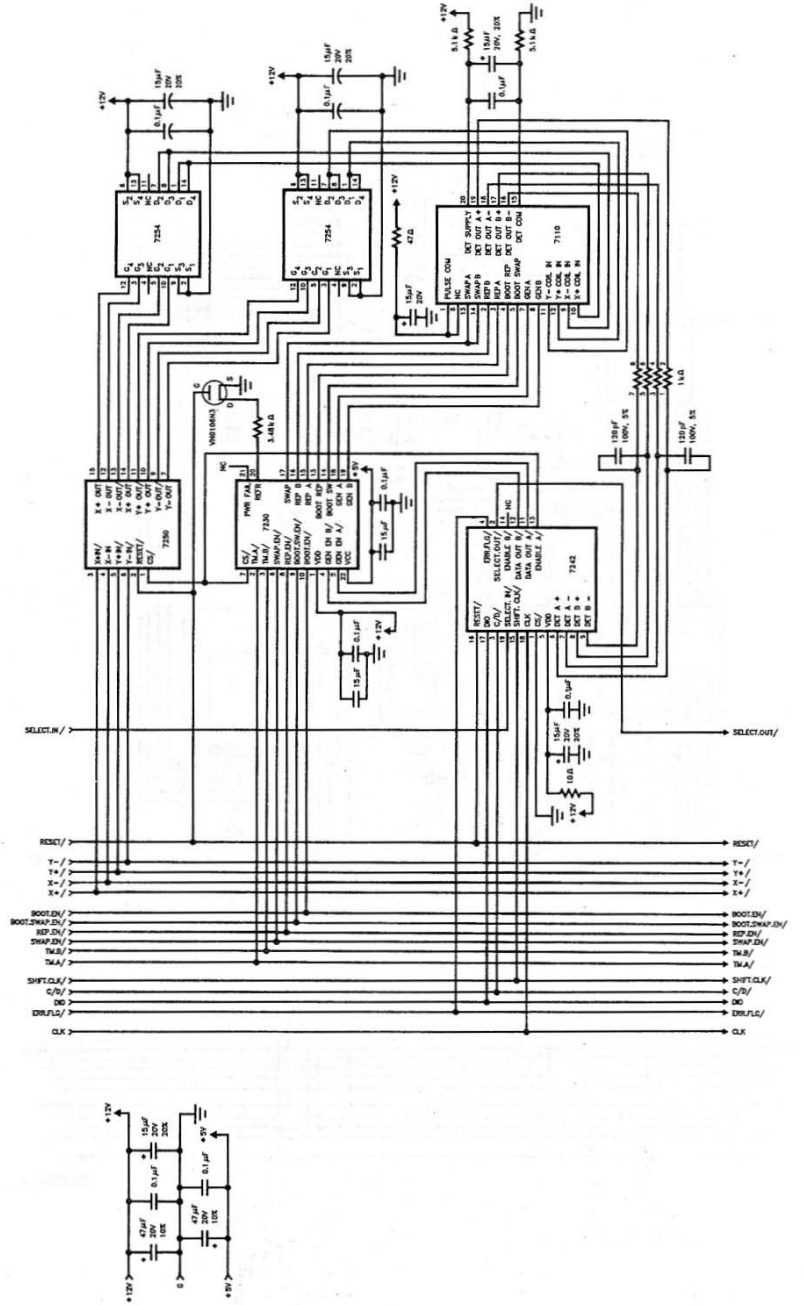

Figure 2b. A Complete Schematic of a Four-Bubble (512 kbyte) Bubble Memory System (Continued)

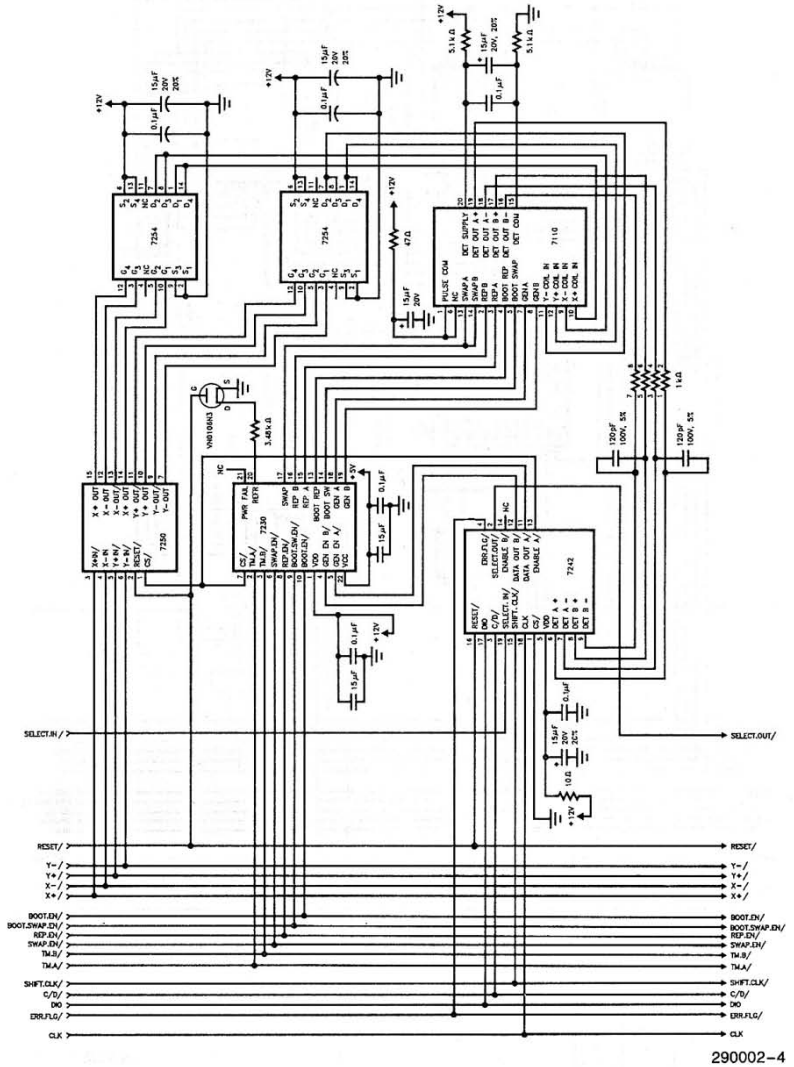

Figure 2c. A Complete Schematic of a Four-Bubble (512 kbyte) Bubble Memory System (Continued)

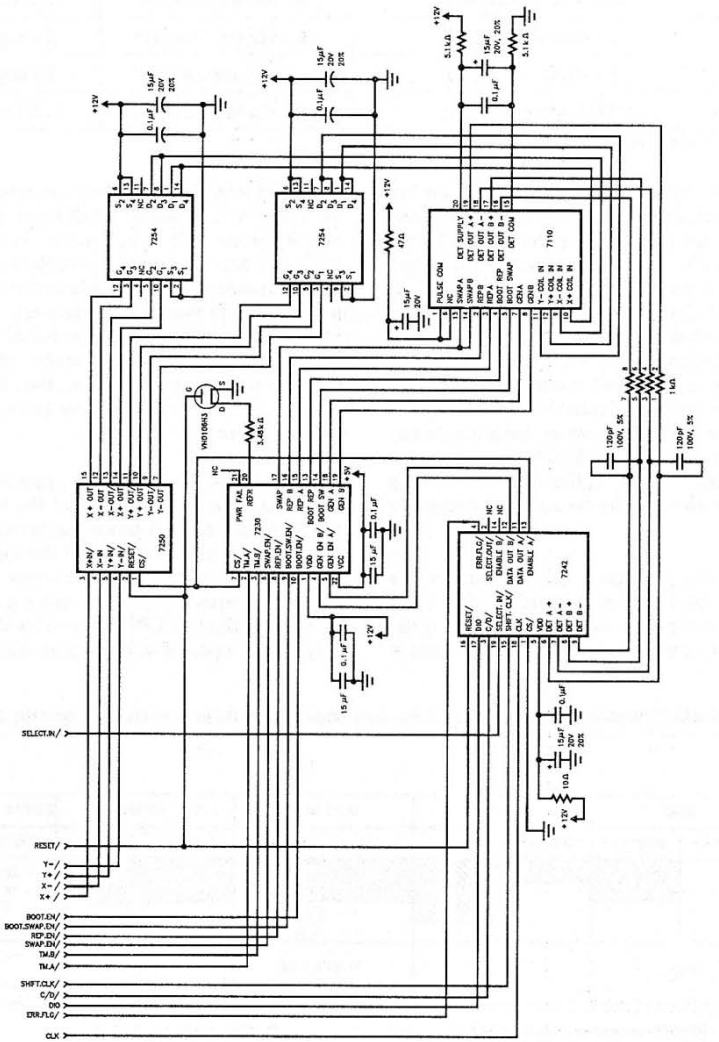

Figure 2d. A Complete Schematic of a Four-Bubble (512 kbyte) Bubble Memory System (Continued)

Table 1. User Data Transfer Rate Requirements

Number of MBMs Operating In Parallel	Maximum Data Transfer Rate between BMC FIFO and the FSAs during Write Bubble Data Commands	Maximum Data Transfer Rate between BMC FIFO and the FSAs during Read Bubble Data Commands	
		*MFBTR = 0	*MFBTR = 1
1	12.5 kbytes/second	50 kbytes/second	12.5 kbytes/second
2	25 kbytes/second	100 kbytes/second	25 kbytes/second
4	50 kbytes/second	200 kbytes/second	50 kbytes/second
8	100 kbytes/second	400 kbytes/second	100 kbytes/second

*Maximum FSA to BMC Transfer Rate Enable Bit

interconnect all the bubble memory banks (such as would only be needed if a single system-wide BMC controller were used) can easily be avoided. In addition, the dedicated controller solution requires only one version of circuit board design instead of two or more. It isn't necessary to design one board for the controller and another for the bubble memory banks. With only one circuit board design, the overall system cost is decreased. And lastly, a dedicated controller solution is both more versatile and more reliable. By using dedicated controllers, each bubble memory bank can be situated on the system bus. There will be no need to create a separate and special bus to buffer signals from the single controller to each of the boards containing the bubble memories.

Adding more bubbles to a given system can have a greater effect than just merely increasing the size of the memory. Through the special hardware built in to the Intel bubble memory support circuitry, the data rate is increased when the BSUs are operated in parallel. Table 1 shows the effect of parallel operation on data rate. An important fact to remember, however, is that the increased data rate is only possible through parallel operation (more than one bubble active at a time) and it is not possible to increase the data rate for multiple bubbles operated serially (only one bubble active at a time). In addition, to operate in parallel, the BSUs must be grouped in powers of two (i.e., two, four, or eight at a time). It is not possible to have three, five, six or seven bubbles operating in parallel.

A point to consider when using parallel operation is the additional overhead required of the host processor. In other words, the host processor must be fast enough to receive data from the BMC at the increased data rate. Table 2 shows parallel configurations which can be supported by various processors using a polled mode data transfer method. A DMA controller should be added to a system to operate at the higher data transfer rates.

Table 2. Data Transfer Speeds and Their Appropriate Processor Data Transfer Method

# OF MBMs	8080		8085		iAPX 86/88		iAPX 186/188/286		SINGLE BYTE TRANSFER	
	MFBTR=0	MFBTR=1	MFBTR=0	MFBTR=1	MFBTR=0	MFBTR=1	MFBTR=0	MFBTR=1	MFBTR=0	MFBTR=1
1									20µs	80µs
2									10	40
4									5	20
8									2.5	10
HIGHEST SPEED VERSION	2 MHz		6 MHz		10 MHz-8086 8 MHz-8088		8 MHz			

INDICATES POLLED MODE FUNCTIONALITY USING HIGHEST SPEED VERSION

INDICATES DMA IS REQUIRED

MFBTR=MAXIMUM FIFO TO BMC TRANSFER RATE ENABLE BIT

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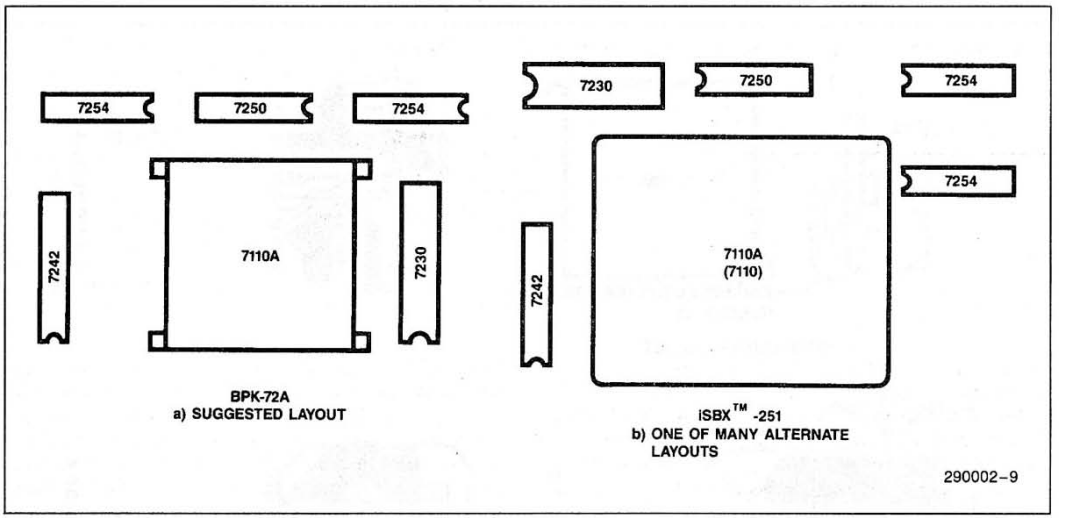


Figure 5. Component Placement Around the 7110A
a) From BPK-72A Board b) From iSBX™-251 Board

SUPPORT COMPONENT PACKAGE LAYOUT

Good circuit layout and correct placement of the support components around the MBM is important to building a reliable bubble memory system. The pin assignments for the Intel 7110A MBM and its support components are arranged to optimize the circuit board layout, to maximize the circuit density, and to ease the task of achieving proper operation. The recommended component layout is shown in Figure 5a since the lengths of the signal traces are minimized. However other methods of package placement are, of course, allowed as shown in Figure 5b.

Other points to consider regarding the components are socketing the 7230 and eliminating solder traces under the 7110A package. The 7230 should be socketed to facilitate re-seeding should the need ever arise in a system which does not use a nucleating pulser. Also, the 7110A package is leaded and is designed to mount flush when soldered to the circuit board. The magnetic shield which surrounds the MBM package is a conducting surface and therefore there should be no traces under the package on the component side. Similarly, the designer should be wary of placing feed-throughs to various board layers under the package as they may be shorted.

THE DETECTOR TO 7242 SIGNALS AND THEIR LAYOUT

The most critical layout area on a bubble memory board exists around the traces between the bubble memory detector output and the inputs to the sense amplifier of the 7242. These signals, which are on the order of five millivolts in amplitude, must be prevented from being corrupted by noise. Though it may appear difficult to isolate low-level signal components in a system with higher-level components such as occur in a bubble memory system, there are some simple design rules to follow to insure reliable operation.

Firstly, the connections between the 7110A bubble detector outputs and the 7242 sense amplifier inputs should be kept as short and direct as possible. Otherwise, long signal traces can act as an "antennae" to receive induced noise from higher-level signals. By keeping the connections short, the "antennae" effect is minimized. This applies to the path through the signal filter as well. Further, the signal filter should be placed as close to the 7242 as possible. By doing so, the detector output signals are kept "clean" before they enter the sense amplifier. Noise is also kept to a minimum by using differential pair lines for the bubble detector signals. Furthermore, the A+ and A− (as with the B+ and B−) traces should be the same length.

Secondly, it is imperative that no digital logic signals cross or come within close proximity of the detector traces. A separation of at least 0.5 inches is sufficient. The circuit board designer should also avoid running digital logic signals parallel to the detector traces. Even in multilayer designs, logic traces should not run below the detector traces.

Thirdly, the X and Y coil drive input traces to the MBM should be separated from the detector signals by as much as possible. The coil drive inputs swing from

Example 1: The BPK-72A, a Two-Layer Solution

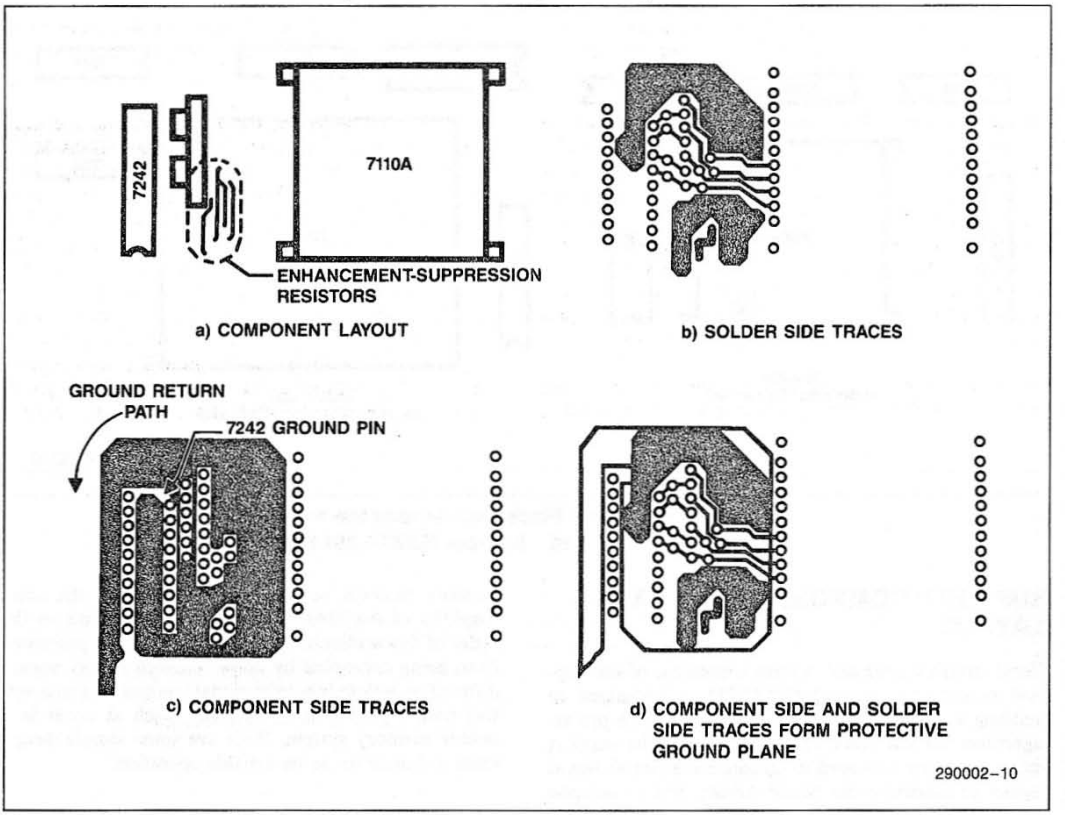


Figure 6. Layout of the 7110A to 7242 Detector Signal Traces on the BPK-72A Board

zero to twelve volts in amplitude at a frequency of 50 kHz. Therefore, by separating these signals from the detector output signals, the circuit board designer can decrease the amount of noise induced onto the detector outputs.

Overall, the majority of noise problems can be solved by electrically isolating the small detector output signals from the rest of the system. Reducing spurious noise on the detector traces improves bubble detection and increases system performance. This is accomplished by providing a ground plane around the detector traces. To implement a ground plane between the 7110A MBM and the 7242 FSA, the circuit board designer can use either a solid or cross-hatched foil pattern depending on his board design preferences.

To more clearly illustrate how to provide a low-noise environment for the detector outputs, this application note presents two approaches to ground plane isolation using examples taken from a two-layer and a four-layer circuit board. The first example is taken from Intel's BPK-72A prototype kit which uses a two-layer circuit board.

As shown in Figure 6a, the 7242 FSA and the signal filter are placed in close proximity to the 7110A MBM. Figure 6b shows the solder side traces that originate at the detector outputs from the 7110A. They travel through the signal filter, and then finally to the 7242 FSA. Surrounding the detector traces is a large foil trace which is part of the ground plane. Figure 6c shows the component side ground plane. It completely surrounds the signal filter and the 7242 FSA. Notice that there are no other signals within 0.5 inches of the detector traces in following the guideline discussed earlier. Finally, Figure 6d demonstrates how the ground planes on the component and solder sides overlap to

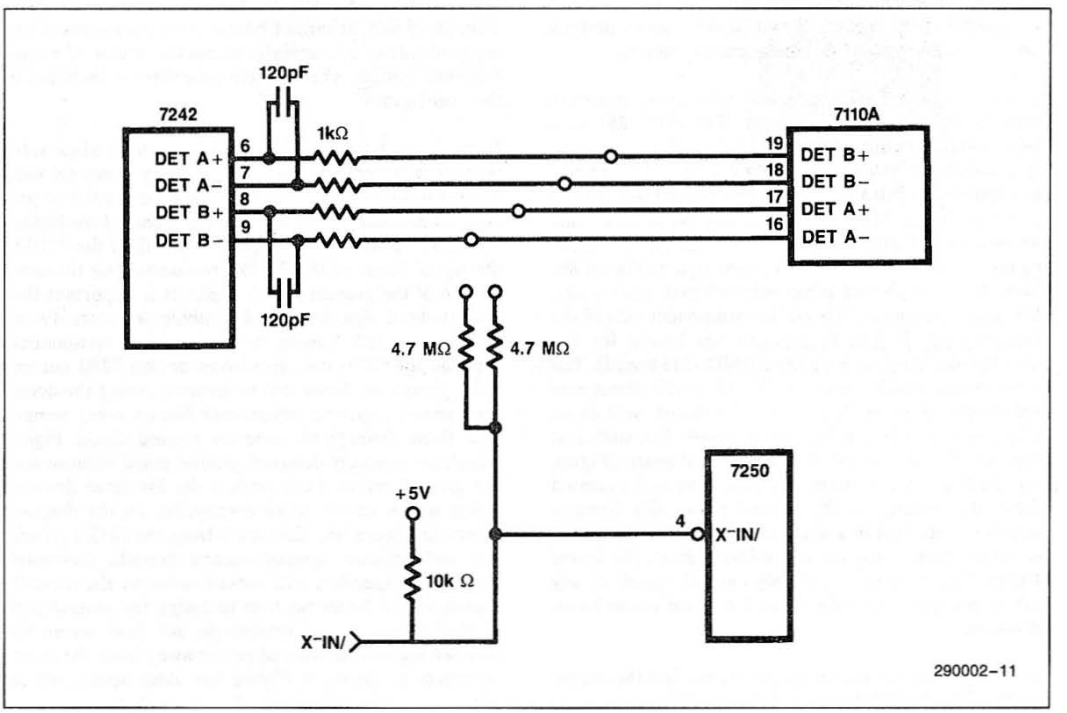


Figure 7. Schematic Detailing the Use of Enhancement-Suppression Resistors

form a protective shield around the low-level detector lines. The shield protects them from noise corruption and this, in turn, increases the data integrity and reliability of the bubble memory circuit board. Also notice that no ground return paths travel past the detector traces. Even the ground pin of the 7242 returns away from the detector circuitry.

The enhancement-suppression resistors as they are so marked in Figure 6 are designed to allow the use of MBMs with bubble detector voltage outputs which are either too high or too low for the 7242's sense amplifier to use. Therefore, by level-shifting these output voltage values, the detector outputs are either enhanced or suppressed, hence the name. The circuit to perform enhancement-suppression is given in Figure 7. However, by utilizing enhancement or suppression, the 7110A MBMs will be interchangeable only with another enhanced or a suppressed MBM because the resistors will be uniquely set up only for either enhancement or suppression. Since enhancement and suppression resistors are used in only special circumstances, most designs can omit the suppression/enhancement circuitry.

Another method to provide a low-noise environment is given in Intel's iSBX-251 board. The iSBX-251 is a double-width Multimodule board containing one megabit of reliable non-volatile memory. The 7242 and signal filter on the iSBX-251 board are located much closer to the 7110A MBM than with the BPK-72A. This can be seen in Figure 8a which shows the part positioning on the iSBX-251 board. The next figure (Figure 8b) shows how the ground plane is interleaved among and surrounds the signal filter on the component side of the circuit board. Figure 8c presents the layout for the power plane (the 2nd layer in the iSBX-251 board). The power plane, which carries +5V and +12V direct current supply voltages throughout the board, acts as an AC grounding plane if the power supply has sufficient capacity. Finally, on the 3rd layer in the board (Figure 8d), the detector traces appear. This layer is the ground plane. By residing in the ground plane, the detector signals are shielded in a situation much akin to a co-axial cable. And lastly, on the solder side of the board (Figure 8e), there are no closely located signals of any sort to interfere with the low-level detector traces located above.

At first glance, the reader might notice that the layout for the 7110A MBM seems different. This is because the iSBX-251 board was designed to accept both the 7110 (which is a leadless part mounted in its own socket) and the 7110A 'Thin-C' part (which has leads and is designed to solder directly to the circuit board). The 7110A 'Thin-C' represents an improvement in that it is smaller, lighter, and more reliable because potential socket contact problems are eliminated by soldering the 7110A to the circuit board.

The iSBX-251 board and the BPK-72A board provide for the enhancement-suppression option should it ever be desired.

The ideal four-layer design is quite similar to the design seen in the iSBX-251 example except that the board layers are placed in a different order. By placing the ground plane (which contains the detector traces) between the ground plane on the component side and the power plane, a coaxial shield is placed around the low-level signals from the MBM as shown in Figure 9. This happens because the power plane acts as an AC grounding plane.

A multi-layer circuit board is suggested for most bubble memory board designs since it represents a more reliable design method than a two-layer circuit board. However, a two-layer board is appropriate for single-bubble systems (such as the BPK-72A) since they typically have a less complicated layout than a multi-bubble system and are sometimes extremely cost sensitive. Though two-layer circuit boards may always seem less expensive, they can actually increase the cost of a multi-bubble system when system reliability is included in the cost figures.

Some precautionary notes about the ground plane solution are in order regardless of how many layers are used in the circuit board. A designer must be careful to prevent other components which are not part of the bubble detection mechanism (i.e., parts other than the 7110A, the signal filter, or the 7242) from occupying the same branch of the ground plane. Again, it is important that the low-level signals from the bubble detectors do not share a ground branch with high-level components such as the 7250 coil pre-driver or the 7230 current pulse generator. Noise can be induced across the detector traces if a ground return path from a noisy component flows through the detector ground shield. Figure 10a shows a poorly designed ground plane because now the ground return path crosses the low-level detector traces which causes noise corruption. In the diagram shown in Figure 10a, the return from the 7242's ground pin and another ground return branch, connected through a capacitor, will induce noise on the detector signals. It is a better practice to design the ground path so that noisy ground returns do not flow across the detector signals but instead return away from the detector traces as shown in Figure 10b. Also notice that no other ground branch shares the same return path as the detector signals. The ground return path through the bypass capacitor shown in Figure 10a does not share the same ground path in Figure 10b and thus the sensitive detector signals in Figure 10b are isolated from noise.

Example 2: The iSBX-251, a Four-Layer Solution

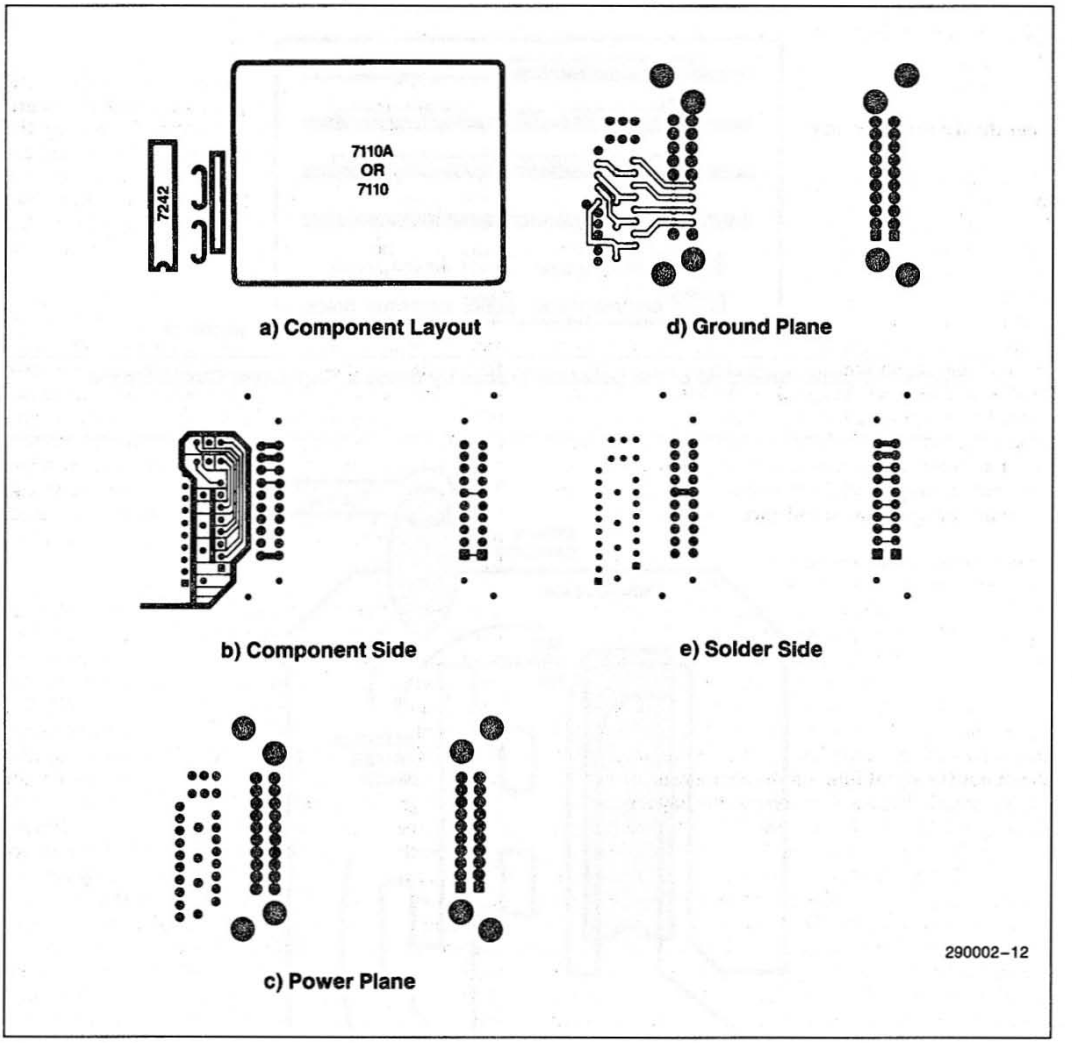


Figure 8. Layout of the 7110A to 7242 Detector Signal Traces on the iSBX-251 Board

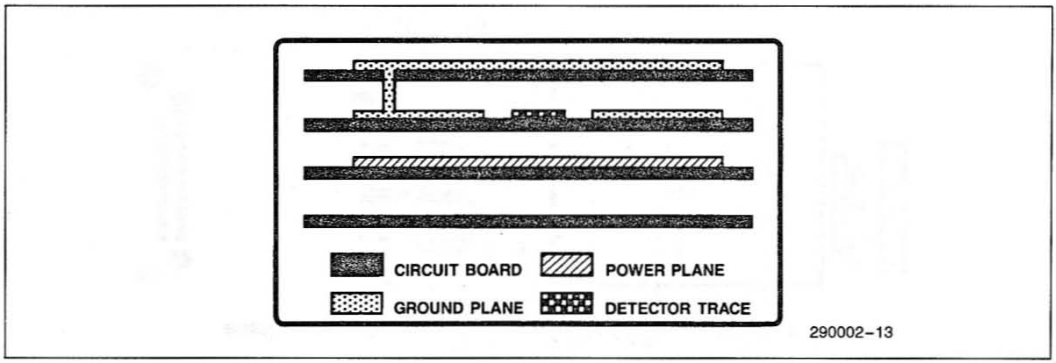


Figure 9. Coaxial Shielding of the Detector Traces by Using a Four-Layer Circuit Board

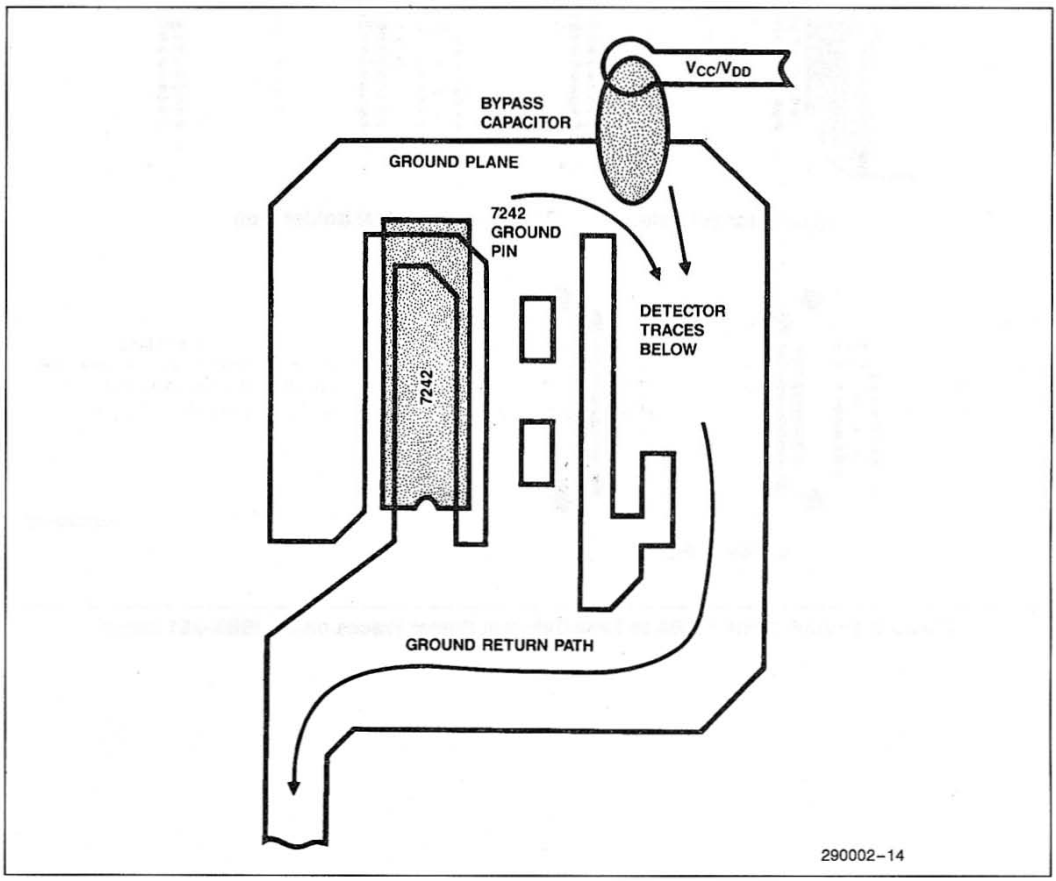


Figure 10a. Example of a Bad Ground Plane.
Notice the Ground Path Over the Low-Level Signals From the Bubble Detectors.

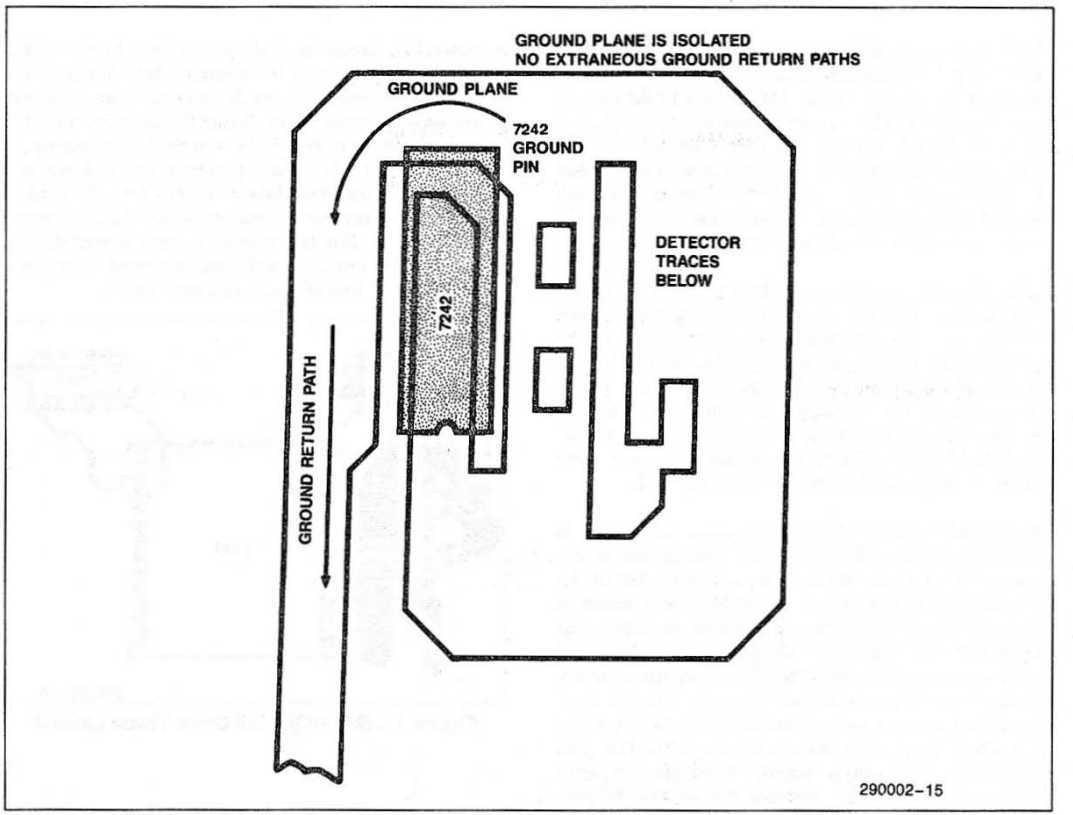


Figure 10b. Example of a Better Ground Plane Than the Example Shown in Figure 10a. The Ground Path Is Now Clear of All Extraneous Ground Signals Thus Reducing Noise.

COIL DRIVE SIGNAL POSITIONING

The X and Y coil drive input traces that go from the two 7254 drive transistor packs to the X and Y coils, contained within the 7110A MBM, should be kept as short as possible. This can be accomplished by placing the 7254 VMOS drivers in close proximity to the 7110A MBM. In addition, these traces should be wide (0.1 to 0.2 inches) and should form a loop of minimum enclosed area. As discussed above, these signals should be kept away from the detector output signals.

Again, the first example of coil drive trace layout comes from the BPK-72A prototyping board. Figure 11 shows how the two 7254s are positioned to either side of the 7110A MBM. The traces shown are located on the solder side of the circuit board. Notice that the X and Y drive signals form the suggested minimum area loop and that they are kept away from the detector outputs. Also, the detector outputs are shielded from the drive signals by the ground plane surrounding 7242.

The second example of coil drive trace positioning is taken from Intel's iSBX-251 board. This layout is presented in Figure 12. When compared with the BPK-72A, the positioning of the two 7254 drive transistors stands out. Both 7254s are positioned to one side of the 7110A MBM as opposed to being positioned above and to either side as with the BPK-72A. Also, the X and Y coil drive traces are connected through both the component and solder layers of the iSBX-251 and not just on a single layer as is done with the BPK-72A (the iSBX-251 is a four-layer board). Since the coil drive signals originate on the opposite side of the detector outputs, they are positioned away from the detector traces as suggested.

POWERFAIL CONSIDERATIONS

A powerfail circuit is built into every Intel bubble memory system in order to safeguard data stored in the MBM from ambiguous conditions that can exist on power-up and power-down. Basically, the powerfail circuitry ensures that all of the system housekeeping is completed before the system powers down and guarantees that no extraneous data is written into the bubble before the support components are ready during a power-up sequence. For this reason, a good powerfail circuit layout prevents any problems associated with power loss (namely loss of bootloops and seeds).

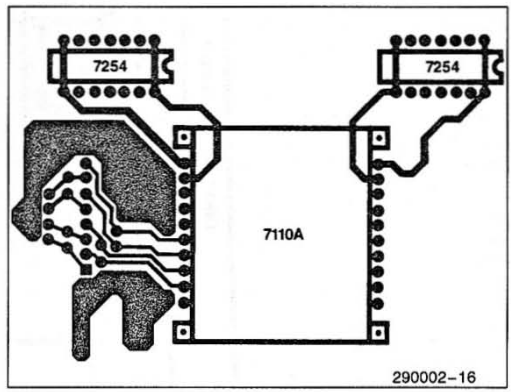


Figure 11. BPK-72A Coil Drive Trace Layout

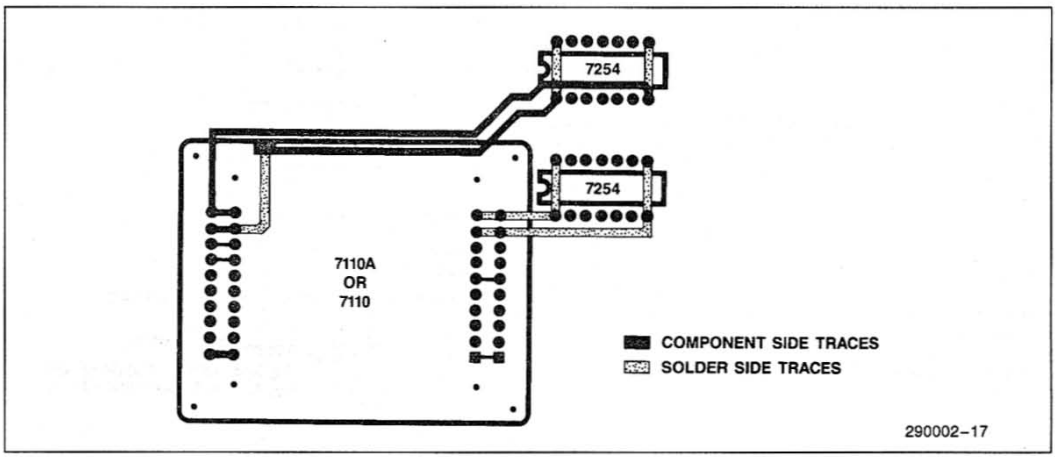


Figure 12. iSBX-251 Coil Drive Trace Layout

A more detailed discussion of the powerfail circuit can be found in the "Powerfail Considerations for Magnetic Bubble Memories Application Note", AP-127 in The Memory Components Handbook. For the purpose of this application note, however, the powerfail circuit is merely a means to insure data integrity.

As with the other components of the bubble memory system, it is important to prevent noise from interfering with proper operation of the powerfail circuit. A schematic of the powerfail circuit is shown in Figure 13. The two 0.01 μF capacitors in the schematic are added to suppress noise found on the powerfail lines. An example of a situation where such capacitors are needed is in a multiple-bubble system employing a two-layer circuit board.

It is also suggested that the designer ensure that the V_{CC} and V_{DD} lines to the 7230's power line monitors are clean and free of glitches. The 7230 is a bipolar device and is capable of detecting power line glitches down to 20 ns. To prevent glitches on the power line from triggering powerfail-induced system shutdown, the designer should include the line filtering circuitry shown in Figure 14 on his circuit board. This additional circuitry is only necessary for the 7230 used in the powerfail circuitry and need not be used on any of the other 7230's in the system. This circuit is included on every Intel bubble memory except the BPK-72A board. For any multiple bubble system or a system which must perform in an inherently noisy environment, the line filter is a necessity. But, since the BPK-72A board is only a one bubble board and uses radial grounding and power distribution to reduce noise susceptibility, it does not use the line filter circuitry.

It is necessary to include only one 7230 per powerfail circuit. By using only one 7230, the designer eliminates the possibility of false powerfail conditions which might be caused by excessive leakage from having multiple 7230 powerfail reset lines wire-ORed together.

The powerfail circuit is capable of driving up to eight BSUs (a complete megabyte) just like 7220. However, a powerfail circuit should be included every time the power originates from a new source (i.e.—two 5V supplies to one board). Therefore, single-board systems require only one 7230 to be actively involved in power fail detection.

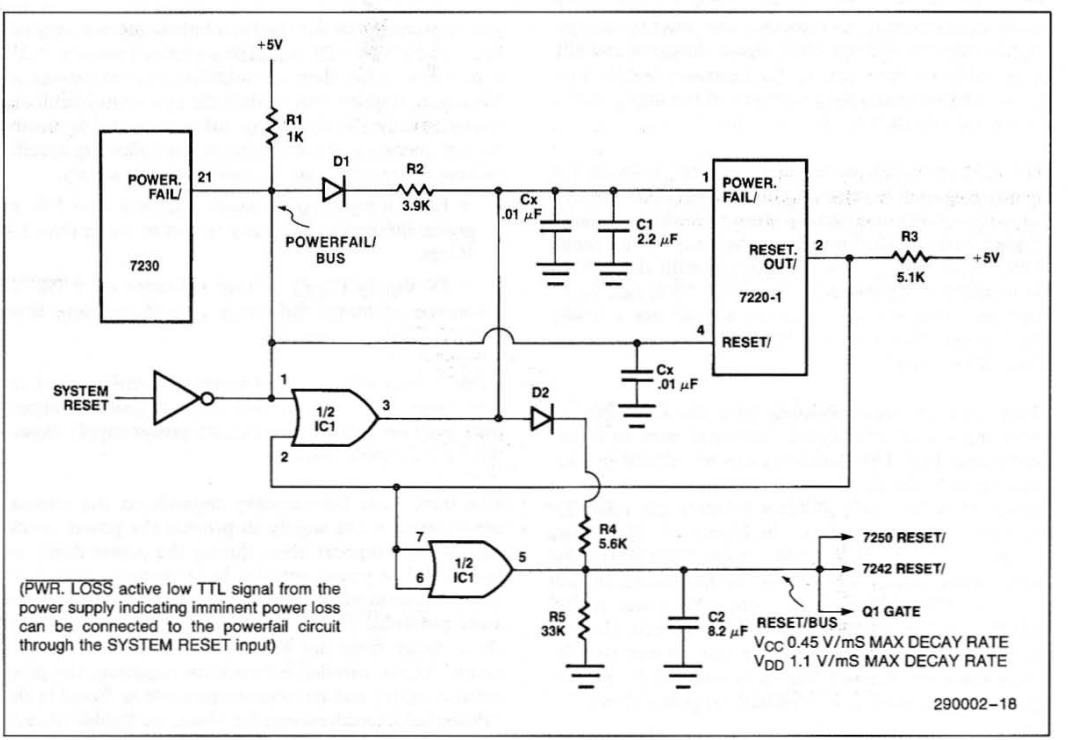


Figure 13. Schematic Detailing the Intel Powerfail Circuit for Bubble Memory

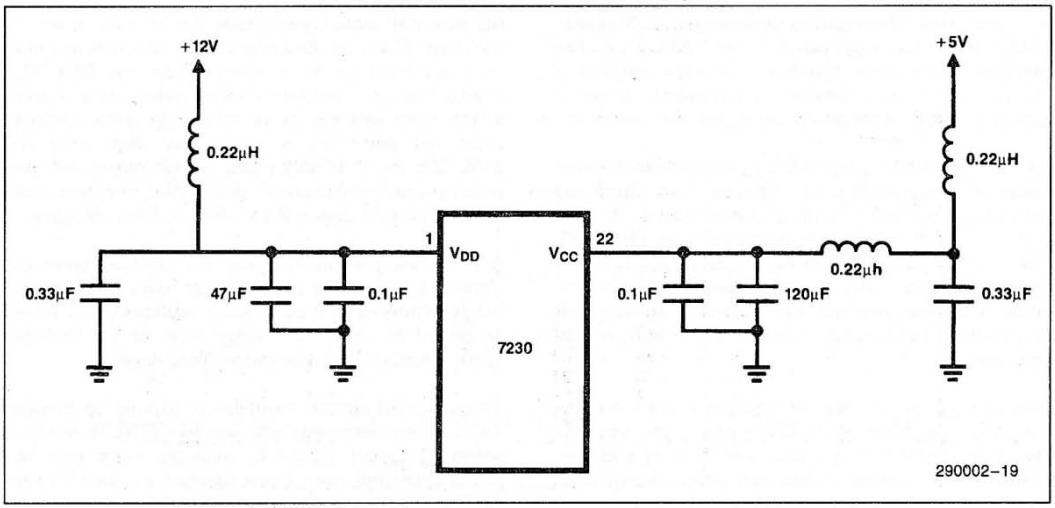


Figure 14. Schematic of the Power Line Filter for the 7230 Used in the Powerfail Circuit

The 75463 TTL line buffer should be located so as to reduce excessive routing of the RESET.OUT signal which can contribute to crosstalk and noise in the system. Ideally, the RESET.OUT signal should be radially branched from the 75463 to the necessary bubble support ICs to avoid coupling with any of the highly active control signals such as the coil drives.

One additional point to consider about the 75463 in the powerfail circuit is regarding high-temperature operation. The 75463 line driver shown in the schematic (Figure 9) is specified only over the temperature range from 0°C to +70°C ambient. For use with the -5 bubble memory components (−20°C to +85°C case operating temperature), the powerfail should use a 55463 which is specified from −55°C to +125°C ambient instead of the 75463.

Many modern power supplies have the capability of providing a TTL level signal which indicates an imminent power loss. This capability can be utilized in conjunction with the Intel powerfail circuitry by connecting an active low open collector driver to the RESET/ input of the 7220 as shown in Figure 13. If at least 130 μs of warning is available to the 7220 BMC, the power supply decay rate spec can be eliminated. In other words, after 130 μs of warning, the power to the bubble memory can drop immediately to zero. However, with this implementation, the Intel power fail circuitry must still be used since it is required for power-up and can be used as a safeguard on power-down.

SYSTEM POWER REQUIREMENTS

The component set for the Intel bubble memory system requires only two DC operating voltages namely +5V and +12V. Also, there are additional specifications on the power requirement in that the powerfail circuit requires specific power decay rates in order to insure proper operation. To summarize, the following specifications are imposed on the system power supply.

- +12V supply (V_{DD}) voltage tolerance of ±5%. A power off/power fail decay rate of no more than 1.1 V/ms.
- +5V supply (V_{CC}) voltage tolerance of ±5%. A power off/power fail decay rate of no more than 0.45 V/ms.

Table 3 gives system and component specific power requirement values. From this table, a system designer can easily determine the necessary power supply capacity for his bubble memory.

The Intel powerfail circuitry depends on the internal capacitance in the supply to provide the power necessary for the support chips during the power-down sequence. Most power supplies have enough internal capacitance to meet the power decay specification for the Intel powerfail circuit. It is extremely important that these decay rates not be violated or data loss might result. Again, detailed information regarding the powerfail circuitry and its requirements can be found in the "Powerfail Considerations for Magnetic Bubble Memories Application Note", AP-127.

Table 3. Bubble Memory Power Requirements (7110A Based Only)

Configuration		Capacity (Bytes)	Power (Watts)					
BPK 72	BPK 70		+5V (Maximum)	+12V (Maximum)	Total Active (Maximum)	Total Active (Typical)	Total Standby (Maximum)	Total Standby (Typical)
1	0	128K	1.92	4.80	6.72	3.90	3.03	1.55
1	1	256K	2.79	9.60	12.39	7.30	4.57	2.60
1	2	384K	3.65	14.40	18.05	10.70	6.11	3.65
1	3	512K	4.52	19.20	23.72	14.10	7.65	4.70
1	4	640K	5.38	24.00	29.38	17.50	9.19	5.75
1	5	768K	6.25	28.80	35.05	20.90	10.73	6.80
1	6	896K	7.11	33.60	40.71	24.30	12.27	7.85
1	7	1024K	7.98	38.40	46.38	27.70	13.81	8.90

Breakdown by Device	Power (Watts)					
	+5V (Maximum)	+12V (Maximum)	Total Active (Maximum)	Total Active (Typical)	Total Standby (Maximum)	Total Standby (Typical)
7110	0	1.740	1.740	1.480	0.440	0.290
7220	1.050	0	1.050	0.500	1.050	0.500
7230	0.235	0.440	0.675	0.390	0.475	0.225
7242	0.630	0.375	1.005	0.500	1.005	0.500
7250	0	0.945	0.945	0.480	0.060	0.030
7254(2)	0	1.300	1.300	0.550	0	0

290002-20

A good quality linear, or switching power supply is a necessity for a reliable bubble memory system. One point to consider is the effect of an over voltage protection circuit (OVP) (also called a crowbar) on the power decay specification given above. In a crowbarred supply, an SCR is triggered by an overvoltage. The SCR then pulls the system power supply to some much lower voltage almost instantaneously to prevent overvoltage-induced component damage. Figure 15 demonstrates how the crowbar, if triggered, can violate the power decay spec and lead to potential data loss. Therefore, crowbarring must be eliminated, or, at worst, prevented until the bubble memory system has completed an orderly shutdown through the powerfail circuitry.

Occasionally, a bubble designer may find the power decay rate specification a bit too constraining and may decide to design a passive power supply decay rate control system to meet powerfail conditions. Such a system will allow the bubble memory system to power down correctly and thus preserve its data. This type of system can provide the power supply decay rate control for cases when either the power to the bubble memory system forms an open (the bubble memory is removed under power) or the supply somehow shorts to ground (the supply crowbars). However, a power supply decay rate control system requires special considerations in its design.

Figure 16 gives a schematic of a general circuit designed to provide for power supply decay rate control. By using this type of LC circuit, the fall rate of the voltage can be controlled. The inductor prevents "current bleedback" into the rest of the system (μP, RAM, etc.) when the power disappear as shown in Figure 17. Thus, the inductor prevents the energy stored in the capacitor C from being pulled to ground along with the rest of the system. This happens since the current through an inductor cannot change instantaneously.

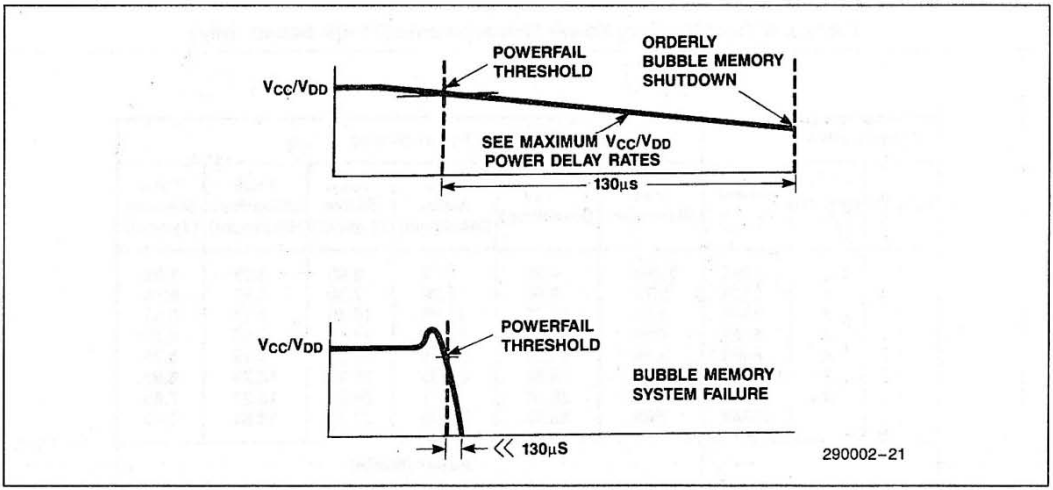


Figure 15. The Effects of Power Supply Crowbarring on Powerfail Conditions

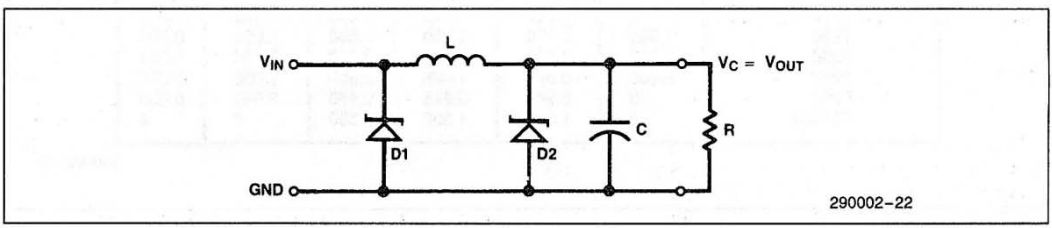


Figure 16. Passive Power Supply Decay Rate Control Circuit

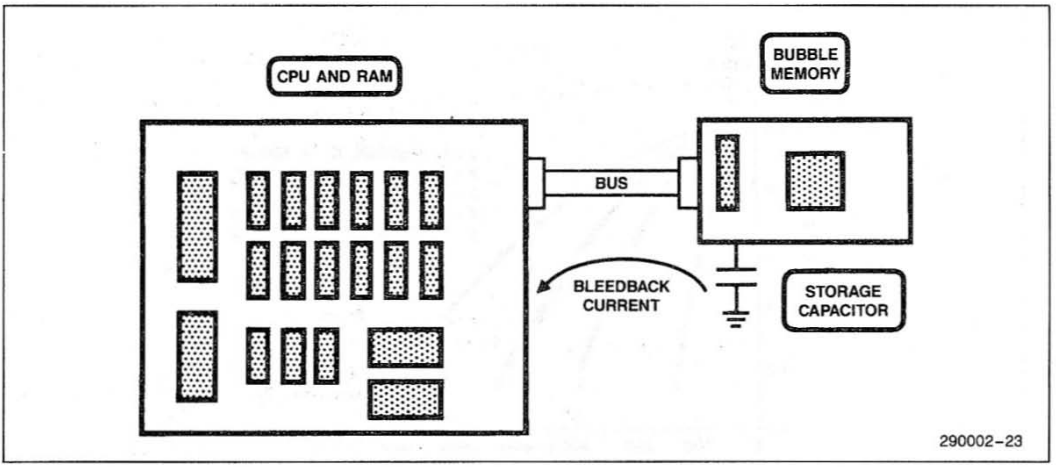


Figure 17. How "Current Bleedback" Happens in a System

Diode D1 has no effect on the circuit in a case when the power supply is shorted to zero. It does, however, take effect when there is an open on the power supply. In this case, diode D1 provides a current path to allow the energy stored in the inductor to supplement the energy stored in the capacitor. Diode D2 merely prevents the output of the circuit from going very negative.

Equation 1 gives the value of the voltage across the capacitor (V_C) over time. Voltage V_i is the initial voltage in the capacitor and, similarly, I_i is the initial current in the inductor, and R is defined as V_i/I_i.

$$V_C = \frac{1}{C} e^{\frac{-t}{2RC}} \left[V_i C \cos \omega t + \frac{I_i}{2\omega} \sin \omega t \right]$$

$$\omega = \sqrt{\frac{1}{LC} - \left(\frac{1}{2RC}\right)^2}$$

Equation 1

Values for L and C can be determined to meet a specific fall rate by using Equation 1 and successive approximation methods. The time parameter (t) is 130 μs as required by the powerfail circuitry to perform the necessary system housekeeping before the power drops too significantly. It is also important to know when a power fail condition will be detected since this will determine the values of V_i and I_i. The powerfail may be signaled by the power supply, thus the supply decay rate control circuitry does not need to hold the voltage for as long. Accordingly, both L and C will be of a smaller value than in a case where powerfail is detected internally by the 7230. For this case, L and C must be larger to maintain the voltage longer (since V_i and I_i will be lower due to the 7230's lower powerfail trip point). Of course, as the LC product increases, so does the time to decay.

For maximum energy storage in the circuit shown in Figure 16, the values of L and C should both be approximately the same. Figure 18 demonstrates the effect of changing L and C with the values for V_i and I_i fixed.

The value of the components is not the only criteria in selecting parts for this circuit. It is imperative that the inductor current rating be sufficient to support the circuit without saturating. If the inductor saturates, it will have no beneficial effect on the circuit and the capacitor will discharge to ground.

Another important consideration is the physical size of the inductor and capacitor. Unfortunately, both components are typically bulky and it may not be possible to incorporate them on a bubble memory board. However, a designer may choose to include the decay rate control circuit in the system backplane.

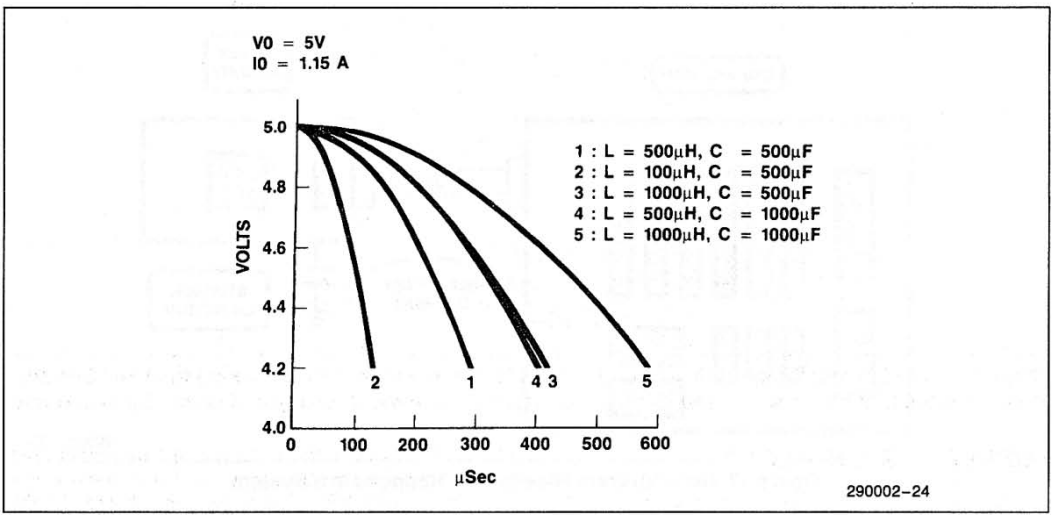


Figure 18. The Effect of L and C on Voltage Decay Rate Using the Passive Power Supply Decay Rate Control Circuit. Initial Voltage and Current Values Are Fixed.

POWER CAPACITORS

Power capacitors, placed around each of the 7254 drive transistors and around each MBM, are specified in the schematic in order to insure reliable operation. They act as a current storage reservoir from which the drive coils can absorb and dump current. Without these capacitors, the inherent board inductance can cause a voltage drop and a subsequent powerfail condition as well as variation in the coil drive amplitudes.

The advantage of using the power capacitors is to confine the peak coil currents to a small area near the coils themselves. The voltage drop across a capacitor can be determined by the simple equation

$$dv = \frac{I_{max}\, dt}{C} \qquad \text{Equation 2}$$

where I_{max} developed on the Y-coil is 750 mA. The time for the current to peak on the Y-coil occurs after 108 degrees of field rotation which happens after 6 μs. The size of the capacitors defined in the schematic is 15 μF. Therefore, the voltage drop that occurs during coil energizing is

$$dv = \frac{750\ \text{mA} \times 6\ \mu\text{s}}{15\ \mu\text{F} \times 2} = 150\ \text{mV} \qquad \text{Equation 3}$$

which is equivalent to a 1.25% drop on the 12V power line. The factor of two appears in the denominator since this value is for a current ramp and not an instantaneous current change. This is, of course, within the 5% tolerance specified for the 12V line.

The power capacitors actually perform another function as well. The drive coils require an almost linear current ramp to drive the magnetic field in the correct manner. Even with the small amount of inductance and resistance in the board, the linear current ramp will take on the form of an LR current curve thus driving the field incorrectly. This effect is shown in Figure 19. By placing the capacitors directly around the MBM coil driver, the amount of undetermined inductance and resistance from the circuit board is minimized.

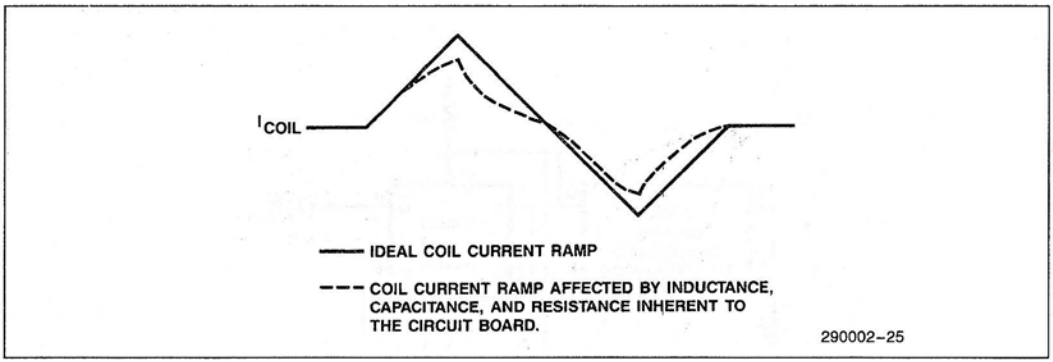


Figure 19. The Current Ramp for the Magnetic Bubble Memory Drive Coils Showing the Ideal Current Ramp and the Effect of Inherent Inductance and Resistance of the Circuit Board on the Current Ramp

BUBBLE SYSTEM CLOCK

Another extremely important aspect of a reliable bubble memory design is the system clock. From a reliability standpoint, the system clock is at least as important as the powerfail circuit. The system clock assures that all the system functions are happening at the correct instances and in the proper sequence. An unstable clock can corrupt the integrity of data stored within the MBM in addition to causing a loss of bootloop or seed.

Further, the clock must start at its specified frequency and not at one of its overtones. Similarly, the clock must start in a stable, well-behaved manner.

The clock specified for a system designed with one megabit parts is 4 MHz ± 0.1% with a 50% ± 5% duty cycle. While it is possible to implement a 4 MHz clock in a variety of ways, it is highly suggested that it be done in the most reliable manner possible. As with any system, the reliability of a bubble memory system is directly proportional to the reliability of each element in the system. Therefore, by using a sub-standard clock, the entire system reliability will be degraded.

As an example, the MTBF (Mean Time Before Failure) of Intel's bubble memory system is specified at 180,000 hours (approx. twenty years of constant operation) when the system is operated at 70 degrees Celsius at 100% duty cycle. However, if the system clock has a MTBF of only 100 hours, then the MBTF of the entire system will drop to only 100 hours.

Figure 20 is an example of an appropriate system clock for use in bubble memory systems. The example is taken from Intel's BPK-72A prototyping board. In this design, an 8 MHz clock signal from a crystal-controlled TTL oscillator is divided by two through a 74S74 dual "D" flip-flop. The flip-flop guarantees that the clock output will have the required 50% duty cycle. A schematic is shown in Figure 20.

SUPPORT COMPONENT DRIVE CAPABILITIES

The drive capabilities of the support components in any system are important and a bubble memory system is no different. The Bubble Memory Controller (BMC) chip, the 7220, is designed to support up to eight BSUs under normal operation with the 7220-1 (0°C to +70°C) and 7220-4 (+10°C to +55°C) components. Table 4 verifies the capability of the 7220 to drive up to eight BSUs.

At present, the 7220-5 BMC (−20°C to +85°C) is specified as being able to drive only four BSUs. This limitation was placed on the 7220-5 due to a worst case analysis of AC loading conditions under full pin loadings. This limitation may soon be removed thus the 7220-5 may be specified to drive up to eight BSUs just like its counterparts, the 7220-1 and 7220-4.

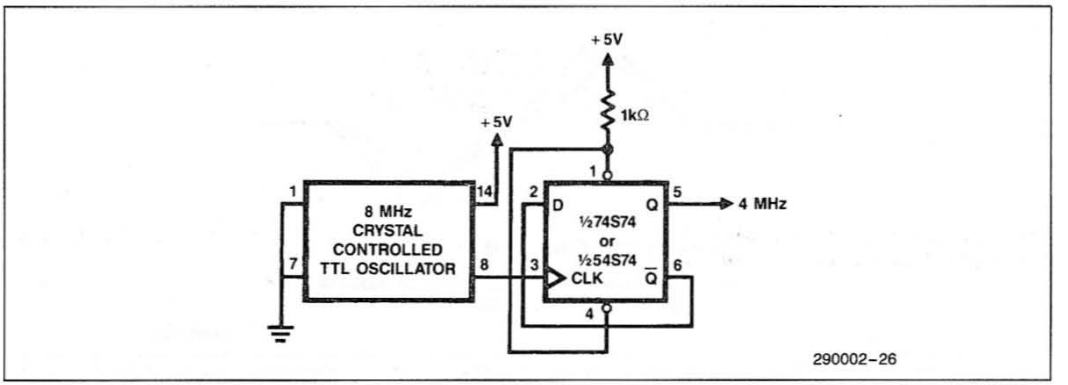


Figure 20. Schematic of a Reliable Clock Design Taken from the BPK-72A Bubble Memory Prototyping Board

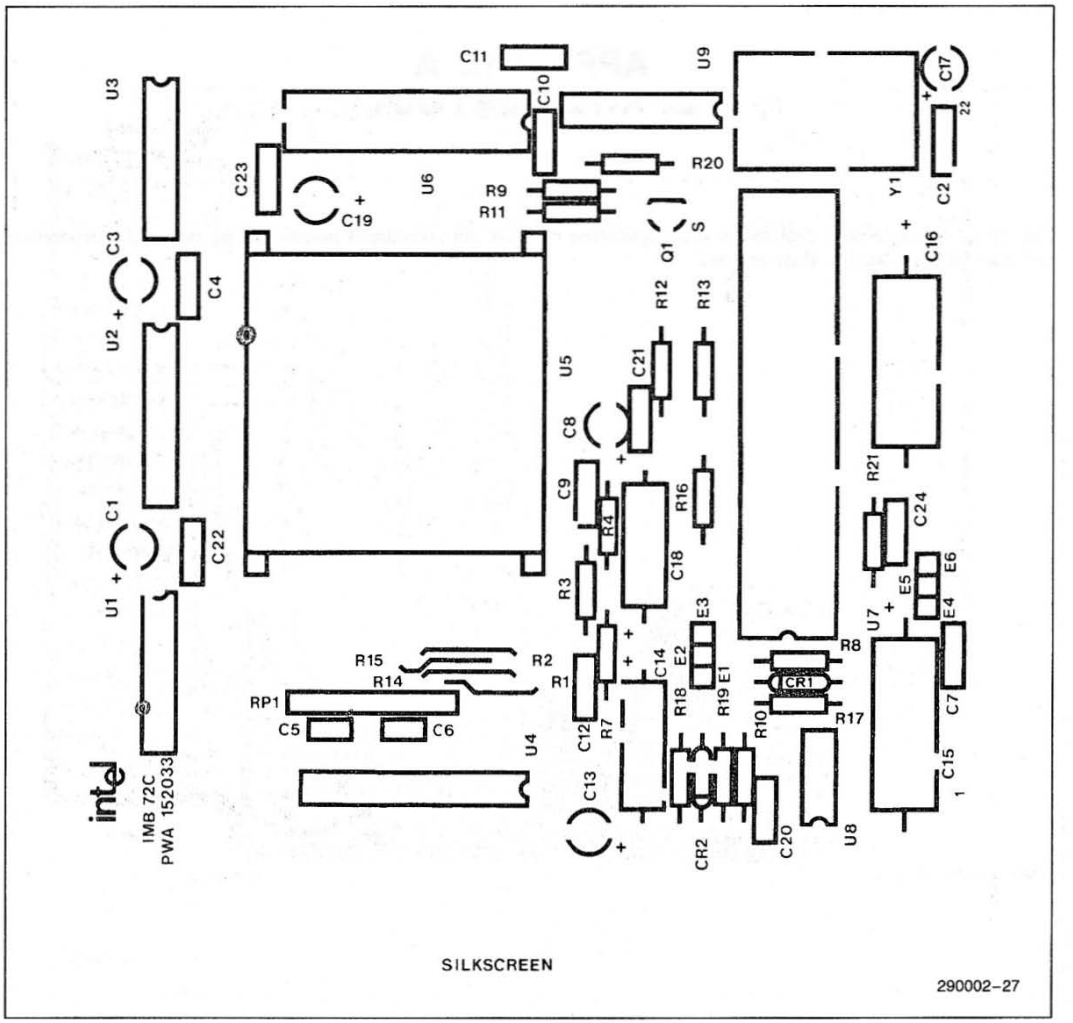
Table 4. Drive Capabilities of the 7220-1 and 7220-4 Bubble Memory Controllers

7220-7230 CONNECTIONS **7230 SIGNALS**	**7220**	**7230**	**RATIO**
TM.A/ TM.B/ REP.EN/ BOOT.EN/ SWAP.EN/ BOOT.SW.EN/	*I_{OL} = 3.2 mA *I_{ON} = 400 μA	$\|I_{IL}\|$ = 400 μA $\|I_{IH}\|$ = 20 μA	8:1 20:1
7220-7242 CONNECTIONS **7242 SIGNALS**	**7220**	**7242**	**RATIO**
DI0 C/$\overline{D}$	*I_{OL} = 3.2 mA *I_{OH} = 400 μA $\|I_{IL}\|$ = 10 μA $\|I_{IL}\|$ = 10 μA	$\|I_{IL}\|$ = 5 μA $\|I_{IL}\|$ = 5 μA *I_{OL} = 3.2 mA *I_{OH} = 400 μA	640:1 80:1 1:320 1:40
SHIFT.CLK/	*I_{OL} = 1.6 mA	$\|I_{IL}\|$ = 5 μA	320:1
7220-7250 CONNECTIONS **7250 SIGNALS**	**7220**	**7250**	**RATIO**
X+.IN/ X−.IN/ Y+.IN/ Y−.IN/	*I_{OL} = 3.2 mA *I_{OH} = 400 μA	$\|I_{IN}\|$ = 5 μA $\|I_{IN}\|$ = 5 μA	640:1 80:1

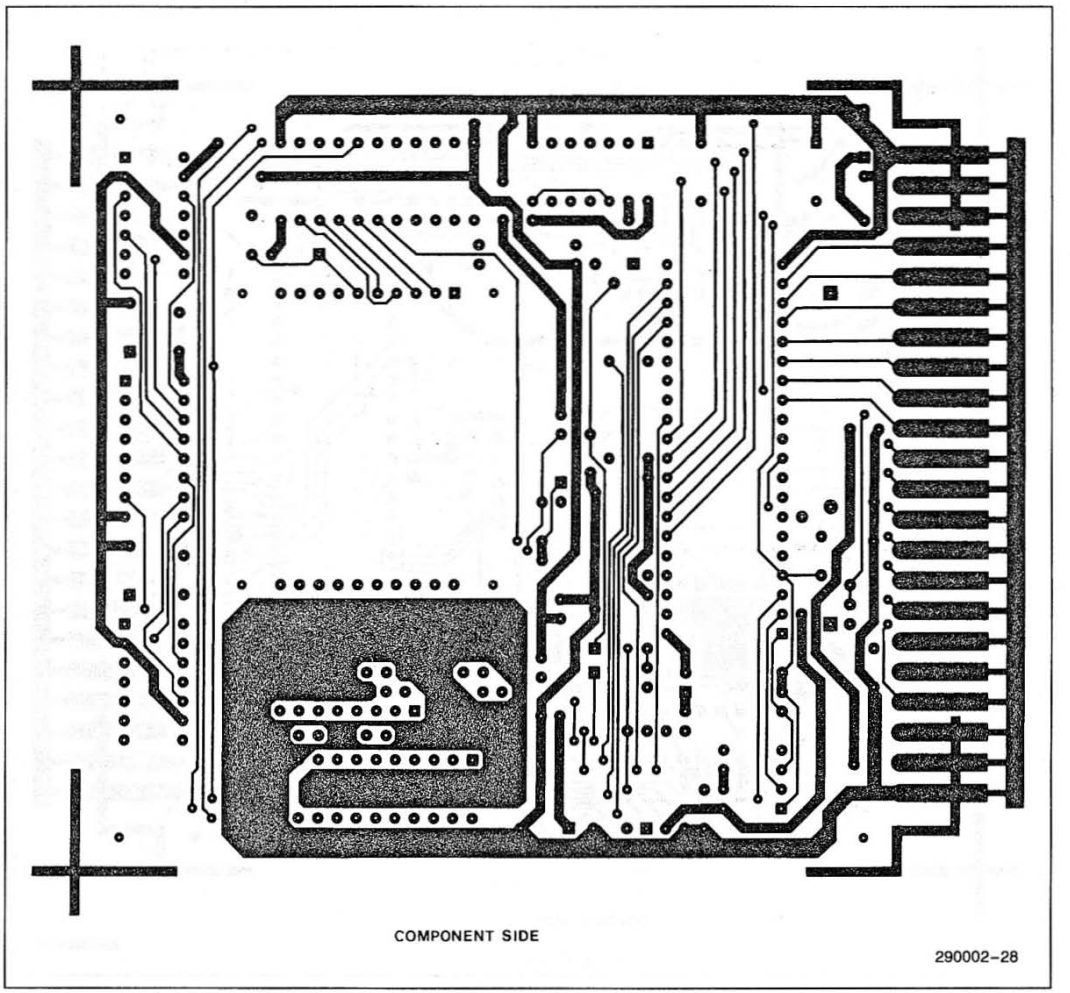
*Indicates Signal Originator

APPENDIX A
BPK-72A LAYOUT

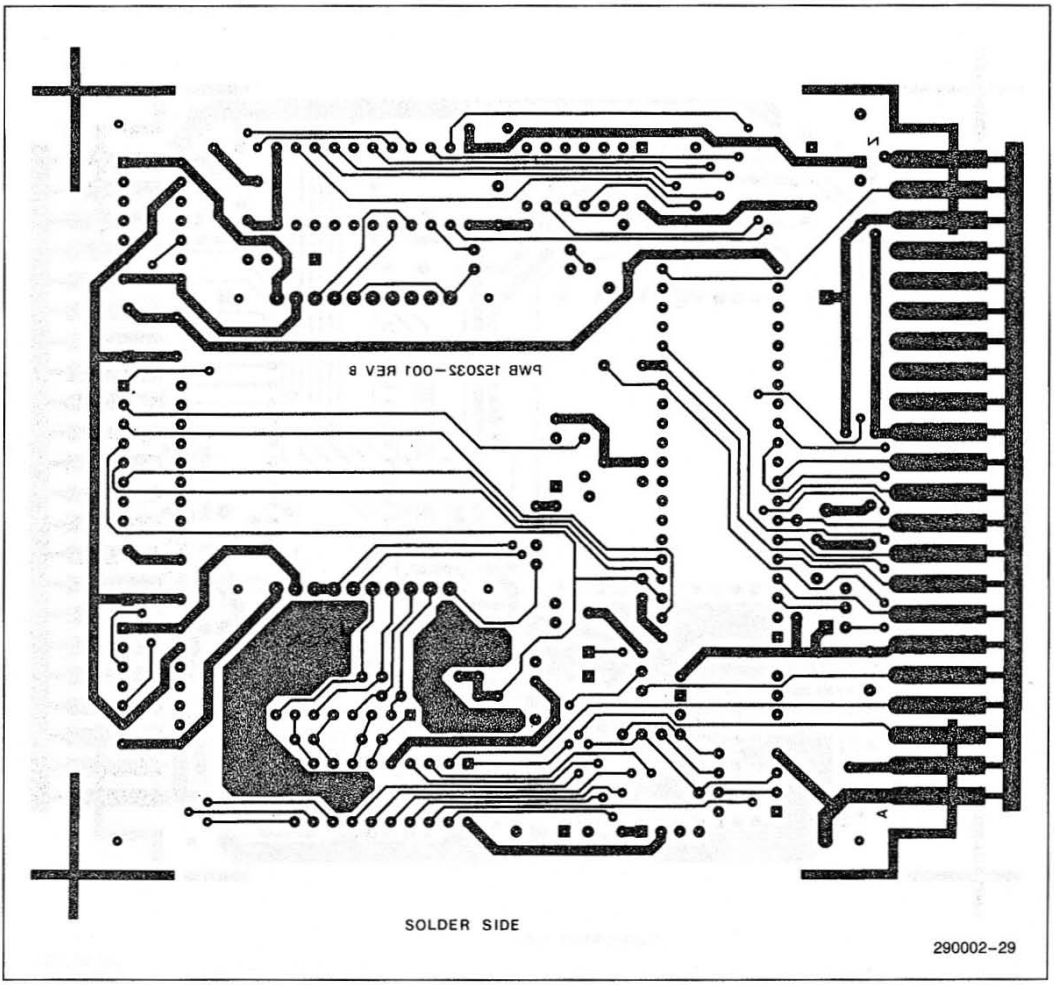
The circuit board layouts depicted in this application note are not considered proprietary by the Intel Corporation and may be duplicated in their entirety.



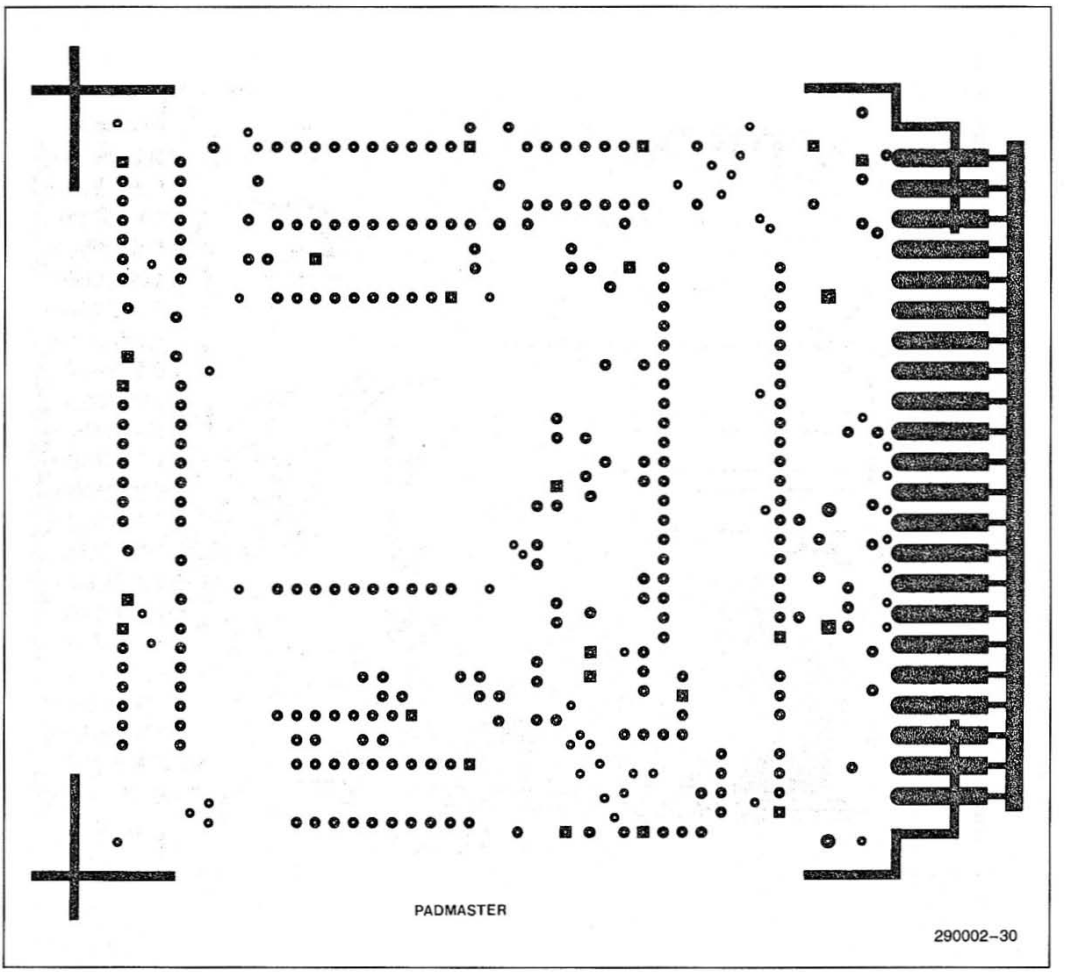
BPK-72A Component Silkscreen



BPK-72A Component Side



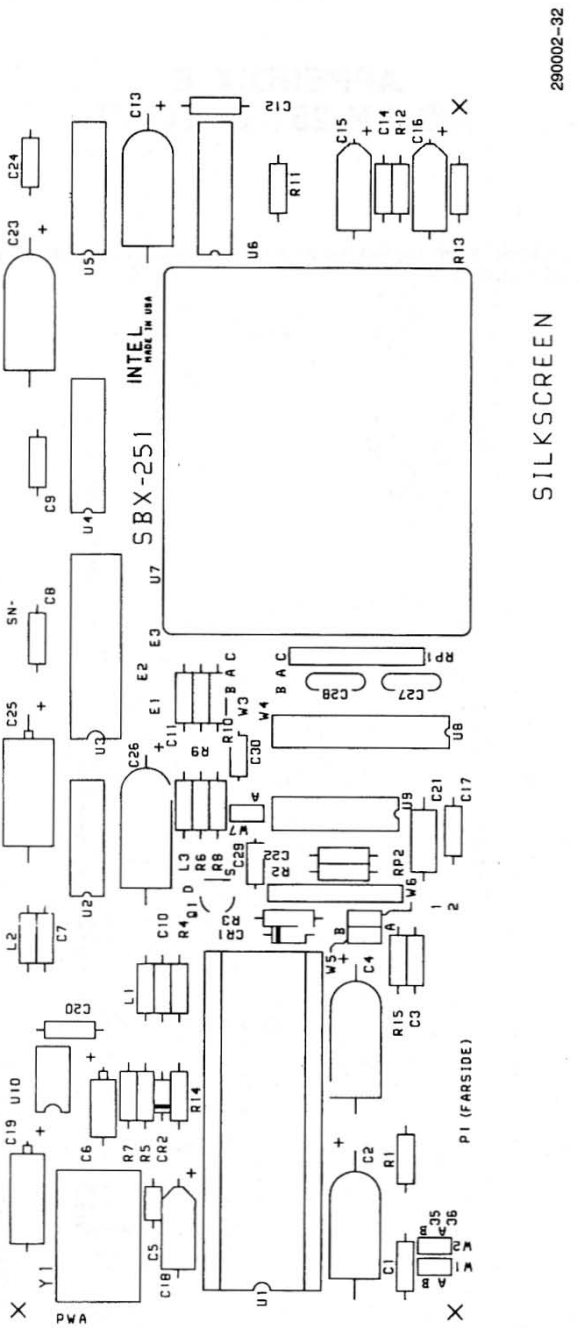
BPK-72A Solder Side



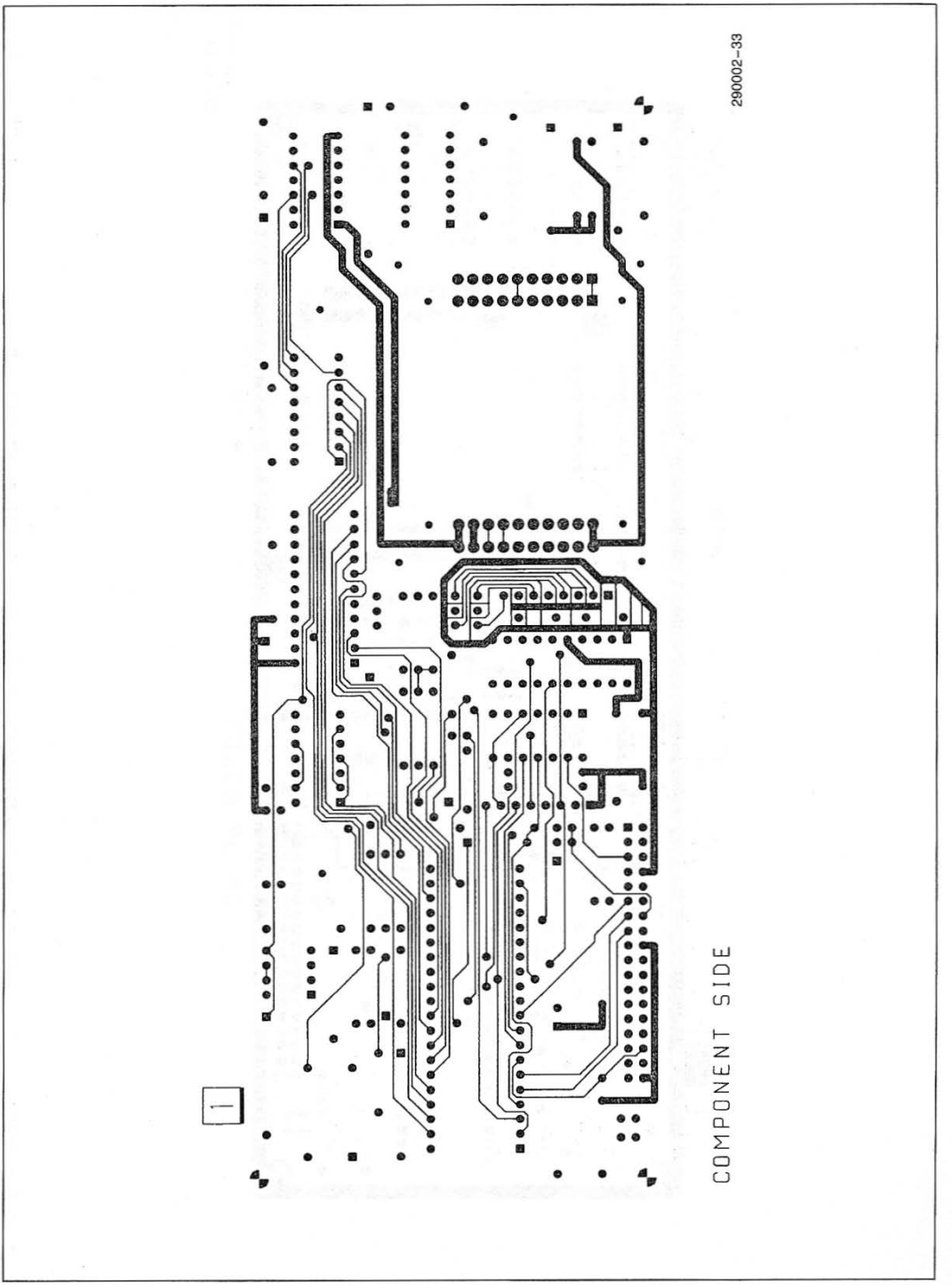
BPK-72A Padmaster

APPENDIX B
iSBX™-251 LAYOUT

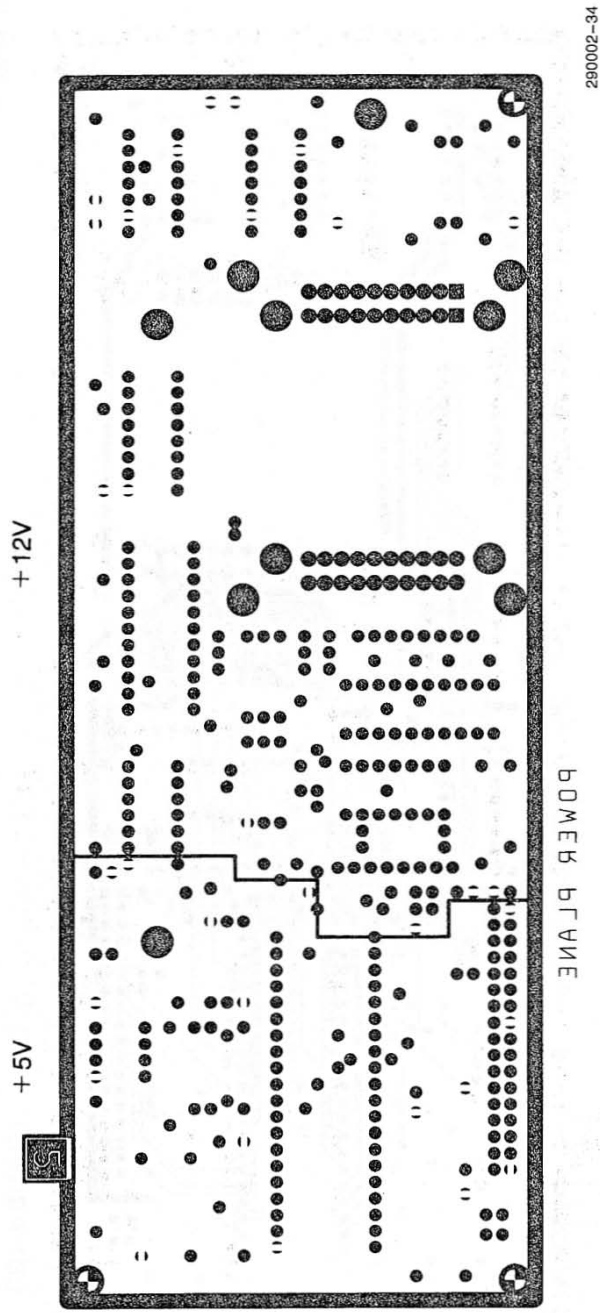
The circuit board layouts depicted in this application note are not considered proprietary by the Intel Corporation and may be duplicated in their entirety.



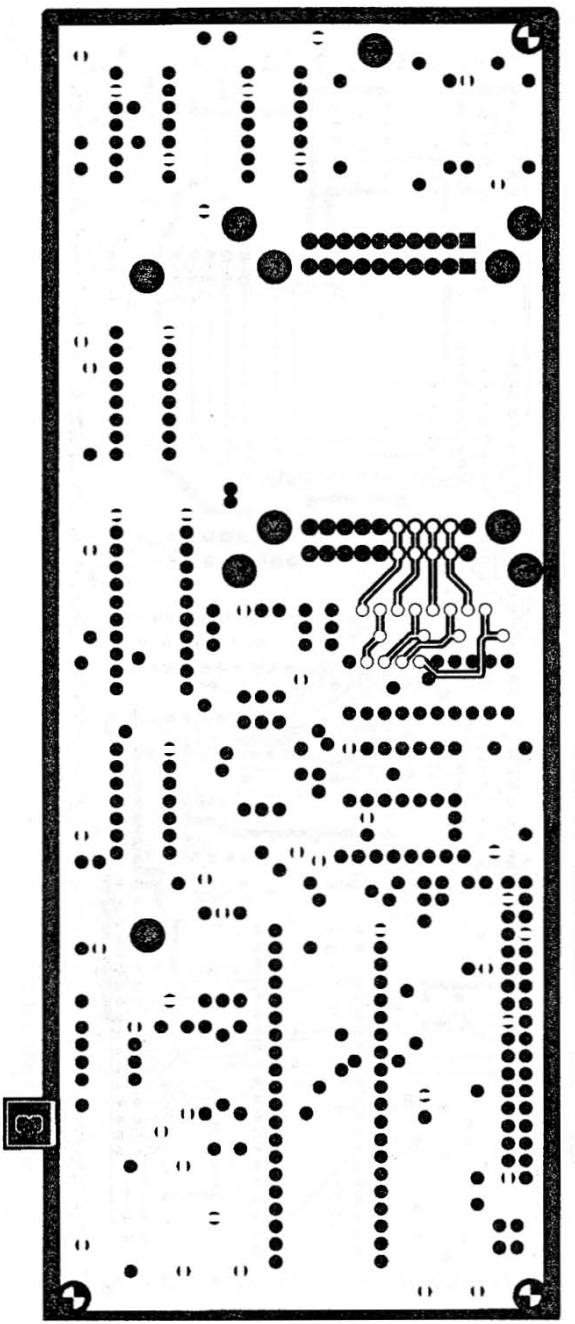
iSBX™-251 Component Silkscreen



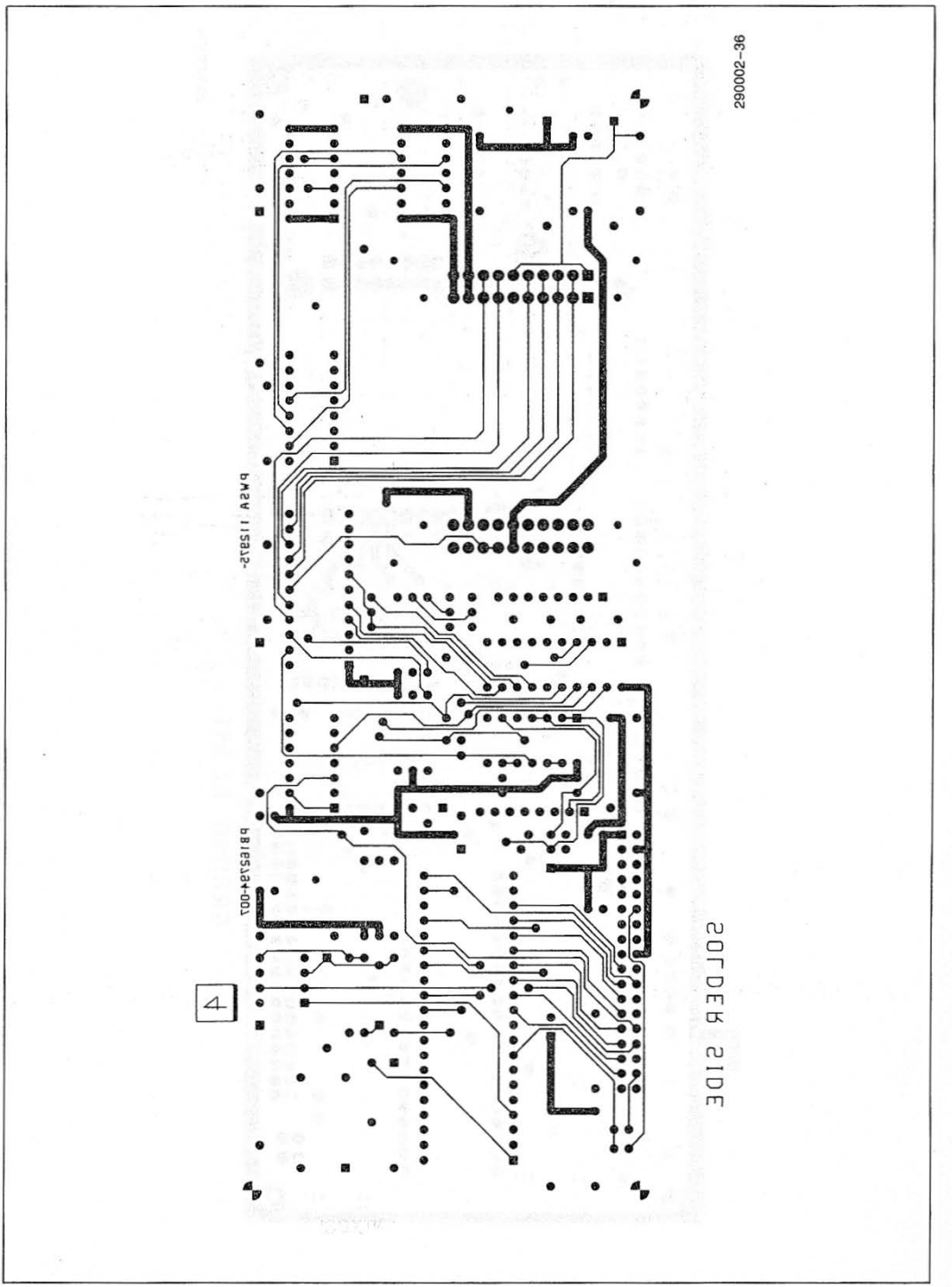
iSBX™-251 Component Silkscreen



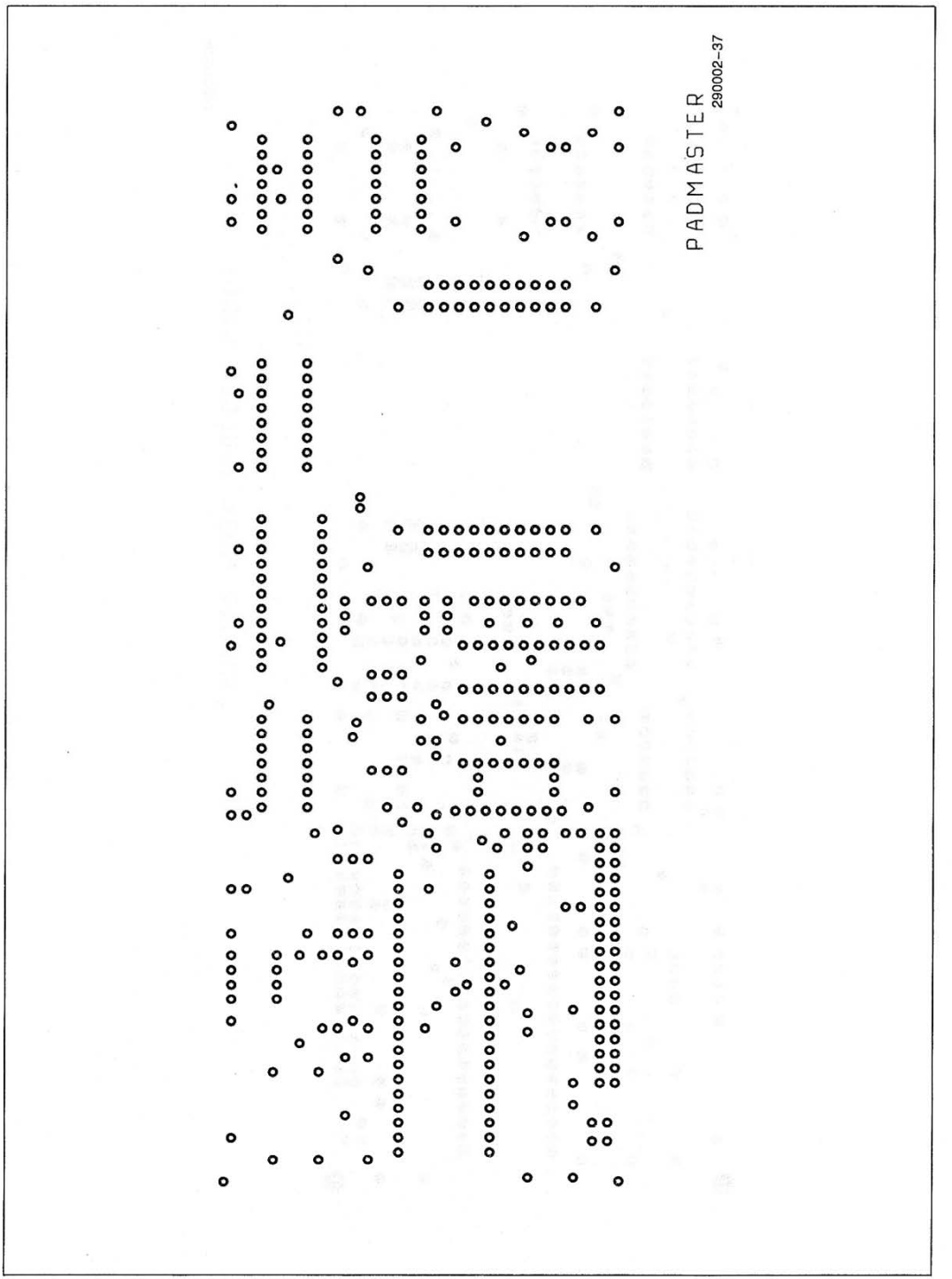
iSBX™-251 Power Plane



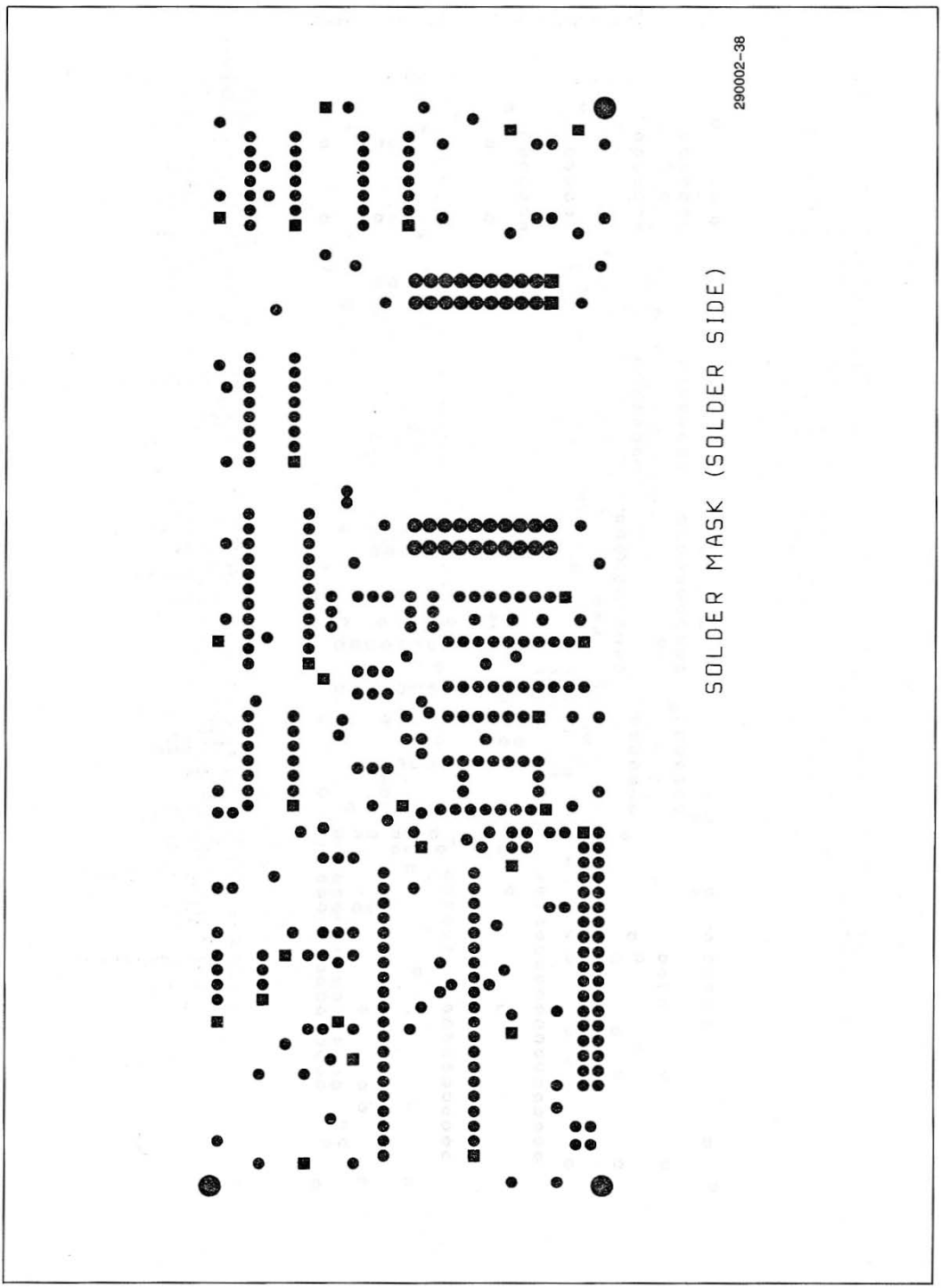
iSBX™-251 Ground Plane



iSBX™-251 Solder Side



iSBX™-251 Padmaster



iSBX™-251 Solder Mask (solder side)

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INTEL INTERNATIONAL CORPORATION Ltd. Swindon, United Kingdom; Tel. (0793) 488 388

INTEL JAPAN k.k., Ibaraki-ken; Tel. 029747-8511

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