

**features**

- Static operation
- 2240-bit capacity
- 64 Characters of 35 bits (5 x 7) or
- 32 Characters of 70 bits (5 x 14)
- TTL compatible
- 700-ns maximum access time
- 7-bit input address
- Single-ended open-drain output buffers

**description**

The TMS 4100 JC/NC series is a family of MOS read-only memories, each with a capacity of 2240 bits. Two organizations are available:

- 1) 64 words of 35 bits (5 x 7)
- 2) 32 words of 70 bits (5 x 14)

The memory is organized to function primarily as a character generator. The seven outputs represent a column in a 5 x 7 dot matrix.

The output word appears as a 5-word sequence on each of the output lines. Sequence is controlled by 5 strobe lines (column select), which feed directly into the buffer section of the memory. By enabling the first strobe line, the first group of 7 bits (first column) is obtained at the output. Then the second, third, fourth, and fifth strobe lines are enabled. The column select can remain fixed while the character address changes, or the character address may remain fixed while the column select changes.

The decoder will accept a 7-bit parallel input. Because only six bits are required in order to decode the 64 input words, the seventh bit may be used as a chip enable. If the memory is organized as 32 words of 70 bits, it is possible to have two chip-enable lines.

The TMS 4100 JC/NC series features static operation. No clocks are required. The output data will remain valid as long as the input address (including chip select) remains unchanged. The V<sub>GG</sub> supply may be clocked to reduce power consumption without affecting access times.

Output buffers are single ended, open drain and allow the wired-OR connection.

The number of words per output is increased by hardwiring together the outputs of different devices. Hardwiring outputs perform the AND function in negative logic.

"TMS 4100 JC" designates a unit mounted in a 28-pin hermetically sealed ceramic dual-in-line package, and "TMS 4100 NC" is the part number for the unit mounted in a 28-pin plastic package.

**logic definition**

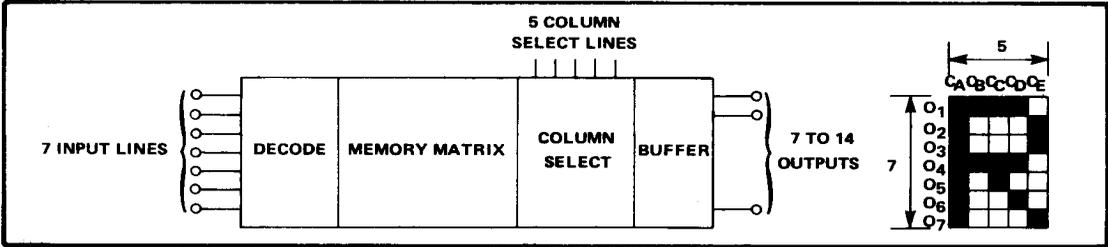
Negative logic is assumed for all inputs.

- a) Logic 1 = most negative voltage (-14 V)
- b) Logic 0 = most positive voltage (0 V)

An output dot is defined as the "on" state of the output MOS transistor and an output blank as the "off" state.

# TMS 4100 JC, TMS 4100 NC SERIES CHARACTER GENERATOR

functional block diagram



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage $V_{DD}$ range (See Note 1)	.....	-30 V to 0.3 V
Supply voltage $V_{GG}$ range (See Note 1)	.....	-30 V to 0.3 V
Data input voltage ranges (See Note 1)	.....	-30 V to 0.5 V
Operating free-air temperature range	.....	-25°C to 85°C
Storage temperature range	.....	-55°C to 150°C

**recommended operating conditions**

CHARACTERISTICS	MIN	NOM	MAX	UNITS
Supply voltage $V_{DD}$	-12	-14	-16	V
Supply voltage $V_{GG}$	-24	-28	-29	V
Input, column select and enable logic 1	-9	-14	-16	V
Input, column select and enable logic 0	+0.3	0	-3	V

Maximum speed of operation will be obtained when operating at the nominal values. The design of the unit permits a broad range of operation that allows the user to take advantage of readily available power supplies (e.g., +12 V, 0, -12 V).

**electrical characteristics (under nominal operating conditions at 25°C unless otherwise noted)**

PARAMETER (See Note 1)	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{(1)}$ Output Blank Current (Note 2)	-14 V applied to output			10	$\mu$ A
$I_{(0)}$ Output Dot Current (Note 2)	-14 V applied to output	1	2		mA
$I_{(0)}$ Output Dot Current (Note 2)	$V_{DD} = -12$ V, $V_{GG} = -24$ V, -12 V applied to output	0.5	1		mA
$V_{(0)}$ Output Voltage for a Dot (Note 2)	$I_O = 0.5$ mA		-1.3	-2.8	V
$V_{(1)}$ Output Voltage for a Dot (Note 2)	$I_O = 1$ mA		-2.5	-6	V
Input and Column Select Leakage Current	-14 V applied to input			1	$\mu$ A
$I_{DD}$ Drain Supply Current			14	25	mA
$I_{GG}$ Gate Supply Current				1	mA
Power Dissipation			250	400	mW
Address Input Capacitance			6	15	pF

- NOTES: 1. These voltage values are with respect to network ground terminal ( $V_{SS}$ ).  
 2. An output dot is defined as the On state of the MOS output transistor. An output blank is defined as the Off state.

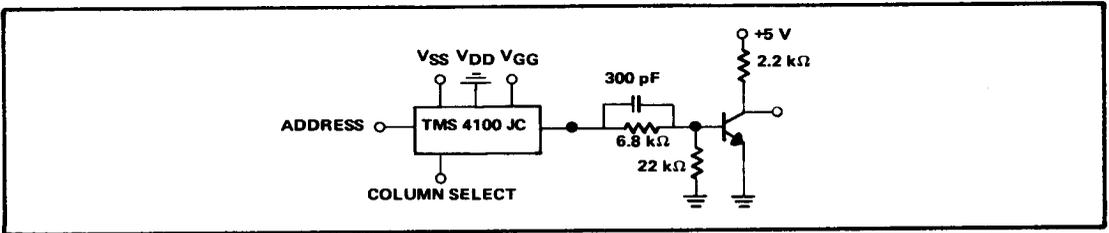
# TMS 4100 JC, TMS 4100 NC SERIES CHARACTER GENERATOR

switching characteristics (at nominal operating conditions and 25°C unless otherwise noted)

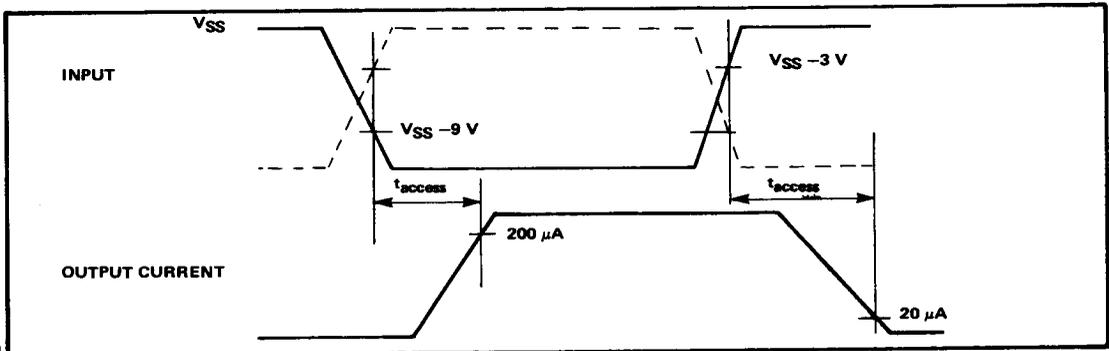
PARAMETER (Refer to Switching Diagram)	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Character Access Time, Bipolar Load			400	700	ns
Character Access Time, Bipolar Load	$V_{SS} = +12\text{ V}, V_{DD} = 0\text{ V}, V_{GG} = -12\text{ V}$		500	700	ns
Column-Select Access Time Bipolar Load			150	300	ns
Column-Select Access Time, Bipolar Load	$V_{SS} = +12\text{ V}, V_{DD} = 0\text{ V}, V_{GG} = -12\text{ V}$		200	350	ns
Character Access Time, Low Power TTL Load			500	850	ns
Character Access Time, Low Power TTL Load	$V_{SS} = +12\text{ V}, V_{DD} = 0\text{ V}, V_{GG} = -12\text{ V}$		600	950	ns
Column-Select Access Time, Low Power TTL Load			200	400	ns
Column-Select Access Time, Low Power TTL Load	$V_{SS} = +12\text{ V}, V_{DD} = 0\text{ V}, V_{GG} = -12\text{ V}$		300	500	ns

## switching circuit and switching diagram

a) Bipolar load



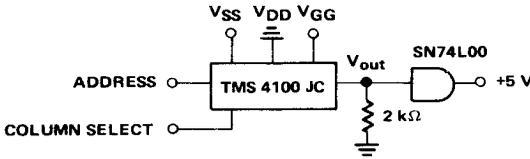
address or column-select input voltage



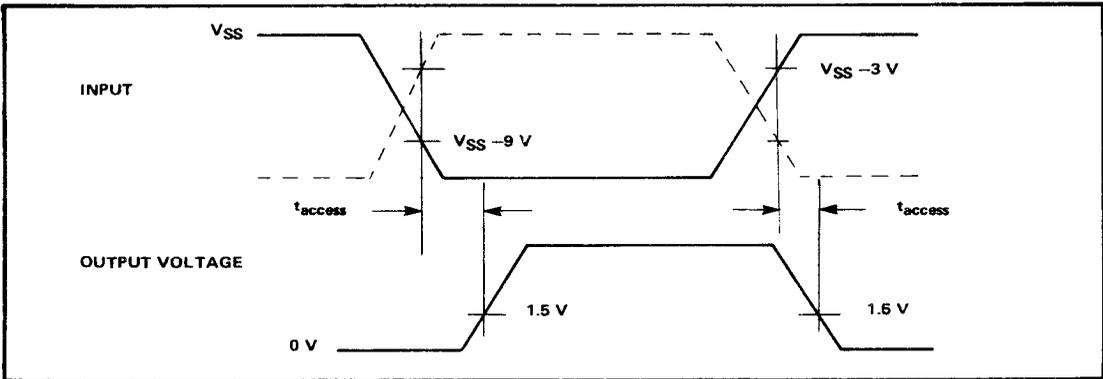
# TMS 4100 JC, TMS 4100 NC SERIES CHARACTER GENERATOR

## switching circuit and switching diagram (continued)

b) Low power TTL load



address or column select voltage



## custom programmed devices

The TMS 4100 JC/NC series is programmed at the gate-oxide stage of manufacturing. Programming charges are reduced to a minimum because only one mask per unique design need be created (gate oxide removal mask). All other processing steps remain the same for all devices. Options available to the customer during programming are:

- memory organization
- character format
- enable logic polarity (or permanently enabled)

The encoding of the gate mask is done by computer to provide a fast, error-free encoding process.

Standard encoding sheets are used. These encoding sheets (SOFTWARE PACKAGE) are available from the TI sales office.

## mechanical data

This device is available in both a 28-pin hermetically sealed ceramic dual-in-line package (TMS 4100 JC) and a 28-pin plastic package (TMS 4100 NC). These packages are designed for insertion in mounting-hole rows on 0.600-inch centers. (See MOS/LSI packaging section.)

14

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# TMS 4100 JC, TMS 4100 NC SERIES CHARACTER GENERATOR

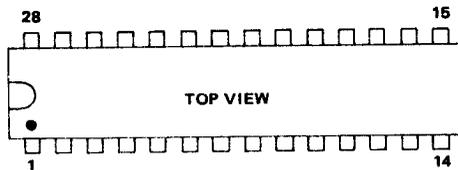
## pin configuration

Depending on the organization of the memory, three pin configurations may be used.

Package Pin Configuration, TMS 4100 JC/NC

PIN NO.	CONFIGURATION		
	A TOTAL OUTPUTS— 7 OR FEWER	B TOTAL OUTPUTS— MORE THAN 7, FEWER THAN 14	C TOTAL OUTPUTS— 14
1	O <sub>1</sub>	O <sub>1</sub>	O <sub>1</sub>
2	NC	O <sub>2</sub>	O <sub>2</sub>
3	O <sub>2</sub>	O <sub>3</sub>	O <sub>3</sub>
4	NC	O <sub>4</sub>	O <sub>4</sub>
5	O <sub>3</sub>	O <sub>5</sub>	O <sub>5</sub>
6	NC	O <sub>6</sub>	O <sub>6</sub>
7	O <sub>4</sub>	O <sub>7</sub>	O <sub>7</sub>
8	NC	O <sub>8</sub>	O <sub>8</sub>
9	O <sub>5</sub>	O <sub>9</sub>	O <sub>9</sub>
10	NC	O <sub>10</sub>	O <sub>10</sub>
11	O <sub>6</sub>	O <sub>11</sub>	O <sub>11</sub>
12	NC	O <sub>12</sub>	O <sub>12</sub>
13	O <sub>7</sub>	O <sub>13</sub>	O <sub>13</sub>
14	V <sub>DD</sub>	V <sub>DD</sub>	O <sub>14</sub>
15	V <sub>G</sub> G	V <sub>G</sub> G	V <sub>DD</sub>
16	I <sub>6</sub>	I <sub>6</sub>	V <sub>G</sub> G
17	V <sub>SS</sub>	V <sub>SS</sub>	I <sub>6</sub>
18	CA	CA	V <sub>SS</sub>
19	CB	CB	CA
20	CC	CC	CB
21	CD	CD	CC
22	CE	CE	CD
23	I <sub>5</sub>	I <sub>5</sub>	CE
24	I <sub>4</sub>	I <sub>4</sub>	I <sub>5</sub>
25	I <sub>3</sub>	I <sub>3</sub>	I <sub>4</sub>
26	I <sub>2</sub>	I <sub>2</sub>	I <sub>3</sub>
27	I <sub>1</sub>	I <sub>1</sub>	I <sub>2</sub>
28	I <sub>7</sub>	I <sub>7</sub>	I <sub>1</sub>

NC — NOT CONNECTED      O — OUTPUT      I — INPUT  
C — COLUMN SELECT



## standard devices

Because certain codes are widely used, TI has created a series of standard devices that are available off the shelf and for which there is no coding charge. The most widely used standard device is: TMS 4103 JC/NC USASCII CODE (See attached character format).

Organization:      64-Character Storage  
                          35-Bit Character Matrix  
                          6-Parallel Character-Address Input  
                          Chip Enabled by Logic 1 Applied to I<sub>7</sub>

# TMS 4100 JC, TMS 4100 NC SERIES CHARACTER GENERATOR

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## standard devices (continued)

### Other Available Standard Circuits:

- TMS 4177 JC/NC and TMS 4178 JC/NC. These two devices are used as a unit to implement a 7 x 10 row output character generator. The two devices are wired OR and are scanned in succession.
  - USASCII Code
  - 64-Character Storage
  - 7-Bit Parallel Input

See attached character format.

- TMS 4179 JC/NC
  - EBCDIC Code
  - 64-Character Storage
  - 7-Bit Parallel Input

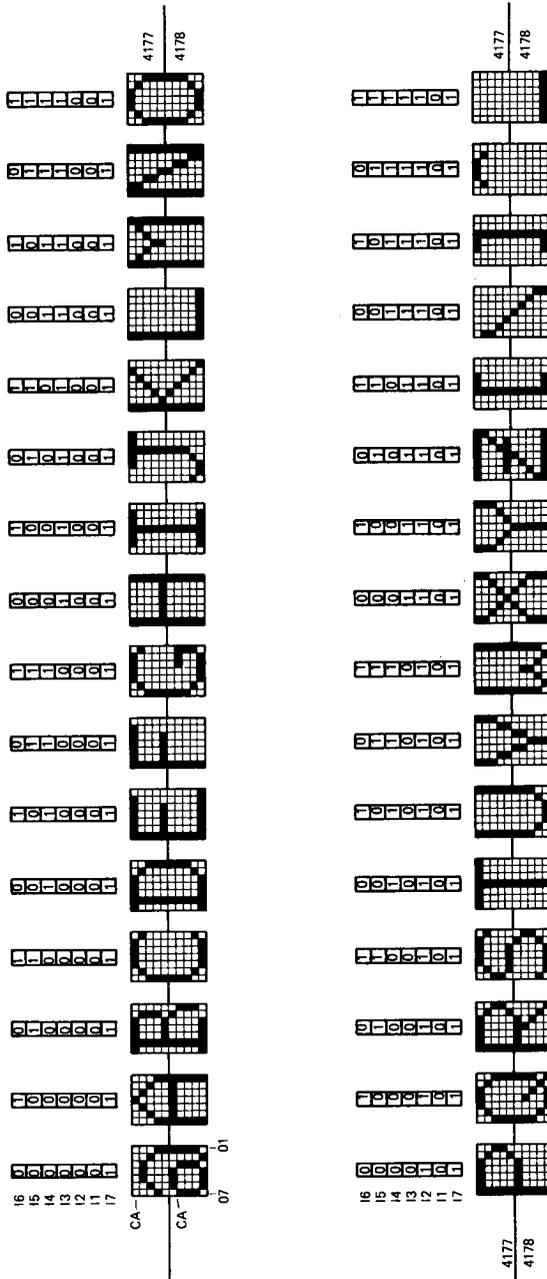
See attached character format.





# TMS 4100 JC, TMS 4100 NC SERIES CHARACTER GENERATOR

TEXAS INSTRUMENTS INCORPORATED  
TMS 4177 JC/NC - TMS 4178 JC/NC (Sheet 1 of 2)  
7 x 10 USASCII CHARACTER DISPLAY







# TMS 4100 JC, TMS 4100 NC SERIES CHARACTER GENERATOR

## TEXAS INSTRUMENTS INCORPORATED MOS COLUMN OUTPUT CHARACTER GENERATOR - TMS 4100 JC/NC SERIES

Coding Sheet 2 of 2

CUSTOMER \_\_\_\_\_ TI CATALOG \_\_\_\_\_  
CUSTOMER PART NO. \_\_\_\_\_ CIRCUIT \_\_\_\_\_

**Coding Symbols**

- 1 - Most Negative Input
- 0 - Most Positive Input
- X - Don't Care Condition

**OPTIONS:**

- 32 Characters - 5 x 14  
I<sub>6</sub> Chip Enable: 1  0
- If 1<sub>7</sub> Must be X
- 32 Characters - 5 x 13  
I<sub>6</sub> Chip Enable: 1  0

- 64 Characters - 5 x 7  
I<sub>6</sub> is 0, Coding Sheet No. 1  
I<sub>6</sub> is 1, Coding Sheet No. 2  
If 1<sub>7</sub> is used as Chip Enable:  
1  0   
X

**For TI Use Only:**

TI Part No. **TMS 4175 JC/NC**  
Engineering Approval \_\_\_\_\_ B/B \_\_\_\_\_  
Decode Deck \_\_\_\_\_ 3 \_\_\_\_\_  
Character Array \_\_\_\_\_ 0.2 \_\_\_\_\_  
Decode Array \_\_\_\_\_ 0.3 \_\_\_\_\_

1	00000000000000	00000000000000	16
2	00000000000000	00000000000000	15
3	00000000000000	00000000000000	14
4	00000000000000	00000000000000	13
5	00000000000000	00000000000000	12
6	00000000000000	00000000000000	11
7	00000000000000	00000000000000	10
8	00000000000000	00000000000000	9
9	00000000000000	00000000000000	8
10	00000000000000	00000000000000	7
11	00000000000000	00000000000000	6
12	00000000000000	00000000000000	5
13	00000000000000	00000000000000	4
14	00000000000000	00000000000000	3
15	00000000000000	00000000000000	2
16	00000000000000	00000000000000	1
17	00000000000000	00000000000000	32
18	00000000000000	00000000000000	31
19	00000000000000	00000000000000	30
20	00000000000000	00000000000000	29
21	00000000000000	00000000000000	28
22	00000000000000	00000000000000	27
23	00000000000000	00000000000000	26
24	00000000000000	00000000000000	25
25	00000000000000	00000000000000	24
26	00000000000000	00000000000000	23
27	00000000000000	00000000000000	22
28	00000000000000	00000000000000	21
29	00000000000000	00000000000000	20
30	00000000000000	00000000000000	19
31	00000000000000	00000000000000	18
32	00000000000000	00000000000000	17

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