8-BIT MOS

AVAILABILITY: Now for 6501, 6502 versions
COST: $20 for 6501, $25 for 6502, 1 pc.
SECOND SOURCE: Synertek, Santa Clara, CA (licensed and in production with MOS Technology masks)

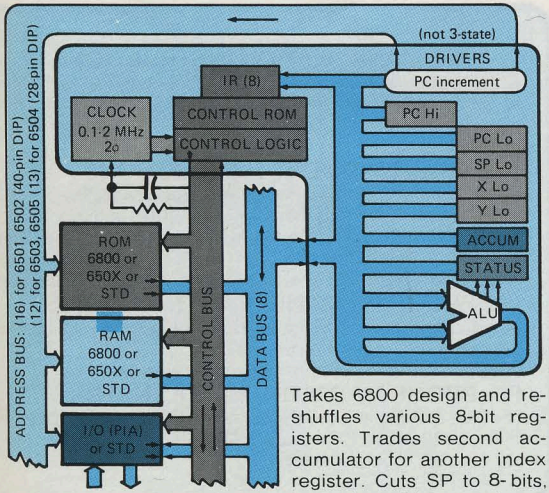
650X

This modification of Motorola 6800 forms a new family that ranges from low cost 28-pin package μP's to 40-pin pseudo-16-bit machines.

MOS Technology, Inc.
950 Rittenhouse Rd.
Norristown, PA 19401
Phone (215) 666-7950

HARDWARE:

NMOS silicon gate with depletion-mode loads; can operate with loose-tolerance 5V supplies. Power drain 250 mW



Takes 6800 design and reshuffles various 8-bit registers. Trades second accumulator for another index register. Cuts SP to 8-bits, but gains address modes.

SOFTWARE:

Although copied from 6800, uses different machine code, so not software compatible. Features greater variety of addressing modes than any previous 8-bit μP.

I—DATA MANIPULATION INSTRUCTIONS

Arithmetic and logical. Decimal mode via control bit in status register. Can operate on locations in memory space (which can be either RAM memory or I/O ports) in same manner as 6800.

II—DATA MOVEMENT INSTRUCTIONS

True indexed addressing, though index offset limited to 8 bits in two CPU registers, X and Y. Short-form addressing to zero page. Has two sophisticated indirect indexed instructions for table handling.

III—PROGRAM MANIPULATION INSTR'S

PDP-11 type conditional branches with signed relative addresses. Edge-triggered nonmaskable interrupt and maskable interrupt. Stack pointer for implementing 256-byte LIFO in external RAM.

IV—PROGRAM STATUS MANIP. INSTR.

Push and pull status register from memory stack.
Set and clear carry, decimal mode, overflow and interrupt bits. (6502 has external input to one status bit, useful for handshaking with peripherals.)

HARDWARE SUPPORT: PC assembly with keyboard entry and display to CRT-based terminal system (MTS). Also available from second source and at least one outside supplier.

SOFTWARE SUPPORT: Cross assembler and emulator, etc. Independent software being prepared by second source.

8 BIT MOS

AVAILABILITY: Now
COST: $65 for CPU in 1-99 qty.; expected to drop to $40-$45 at 5-10k volume in '76.
SECOND SOURCE: AMI (S6800), MOS Technology, Synertek

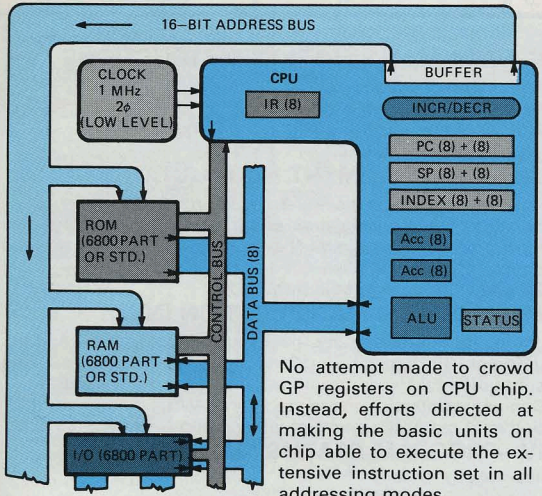
6800

Goal was to combine as much of the capability of a modern minicomputer into building blocks resembling an LSI version of a logic family.

**Motorola Inc., Semiconductor Div.,
5005 E. McDowell Rd.,
Phoenix, AZ 85008.
Phone (602)244-6900**

HARDWARE:

NMOS silicon gate at single +5V supply with compatible memory and I/O chips.



No attempt made to crowd GP registers on CPU chip. Instead, efforts directed at making the basic units on chip able to execute the extensive instruction set in all addressing modes.

SOFTWARE:

Copied from the PDP-11 set as closely as is possible with a shorter word-length machine. Execution times from 2-5 μsec.

I—DATA MANIPULATION INSTRUCTIONS

Arithmetic and logic.
Instructions to take advantage of two accumulators.

II—DATA MOVEMENT INSTRUCTIONS

Can reach the first 256 locations of memory with short instructions.
Can list-process efficiently with the Index Register.
Relative addressing allows data relocation.

III—PROGRAM MANIPULATION INSTR'S

Has the PDP-11 Branches and Conditional Branches. Unlimited subroutine nesting via stack pointer addressing LIFO stacks in RAM.
Does not have vectored interrupt, but can achieve function with software.

IV—PROGRAM STATUS MANIP. INSTR.

Instructions for storing status register.

HARDWARE SUPPORT: Various levels of pc board and console aids.

SOFTWARE SUPPORT: Cross assembler, interactive simulator, debug with a PL/M type hi-level language.

8080/8080A

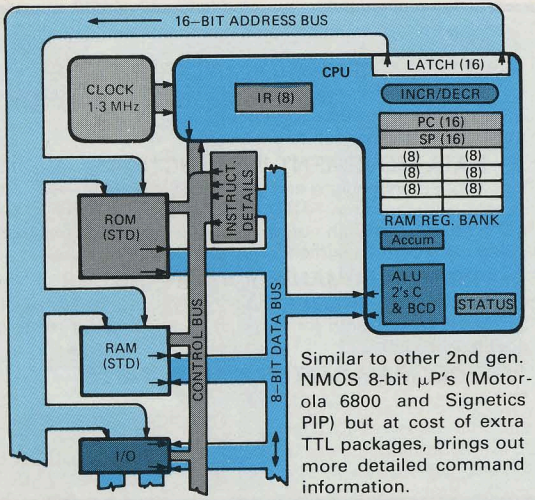
AVAILABILITY: Now
COST: From $29.95 in 100 qty., depending on source. Expected to drop to $15 in high volume in '76.
SECOND SOURCE: AMD (9080A), T.I. (TMS-8080), NEC Microcomputers (8080, 8080A and 42-pin 753).

8080 is the most widely accepted μP. Holds up well in benchmark competitions with newer 8-bit machines. "A" version features improved interrupt.

**Intel Corp.,
3065 Bowers Ave.,
Santa Clara, CA 95051.
Phone(408) 246-7501**

HARDWARE:

NMOS dynamic 2-phase logic using multiple power supplies (±5V, +12V) and hi-level clock.



Similar to other 2nd gen. NMOS 8-bit μP's (Motorola 6800 and Signetics PIP) but at cost of extra TTL packages, brings out more detailed command information.

HARDWARE SUPPORT: Widest selection of any μP, ranging from board assemblies by prime and second sources, to full development systems from prime source and at least a half-dozen independent suppliers

SOFTWARE:

Three co-equal full-width (16-bit) pointer registers allow efficient addressing of full 65k of memory space, despite limited addressing mode.

I—DATA MANIPULATION INSTRUCTIONS

Arithmetic and Logic.
BCD arithmetic.
Double-precision operations (instructions string two data bytes together as 16-bit word).

II—DATA MOVEMENT INSTRUCTIONS

Uses three pairs of so-called GP registers as pointers in CPU RAM bank to address low- and high-order bits of 16-bit memory address. Can do multiple indexing with these, but takes additional steps compared to classical index register concept.

III—PROGRAM MANIPULATION INSTR'S

Uses stack pointer (SP) to create LIFO stacks in external RAM for unlimited subroutine nesting.
All GP registers can be incremented and decremented.
Multiple interrupt capability.
Bus controls allow adding DMA.

IV—PROGRAM STATUS MANIP. INSTR.

Software access to status register.

SOFTWARE SUPPORT: Has made heavy investment in developing a high-level language (PL/M) for this machine.

AVAILABILITY: Now
COST: $40 for 4-6V sets; $56 for 3-15V sets
SECOND SOURCE: Advanced Memory Systems (may also do NMOS version as well as SOS versions)

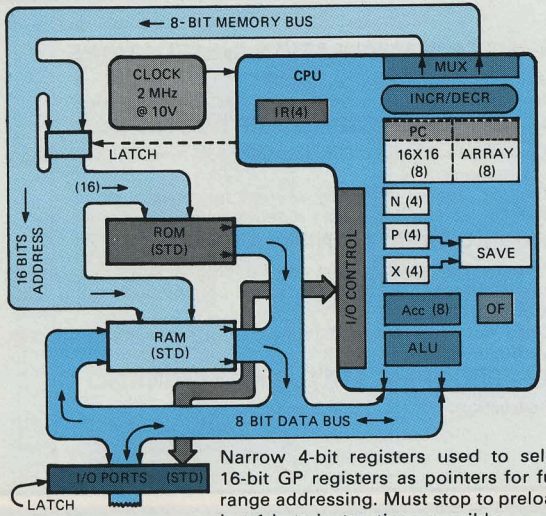
CDP 1801

Formerly called COSMAC, the CDP1801 makes extensive use of pointer-based addressing. CMOS provides low power, −55 to +125°C operation.

RCA Solid State Div.
Route 202
Somerville, NJ 08876
Phone (201) 722-3200

HARDWARE:

Initially CPU is supplied in 2-chip sets using standard 4000A CMOS process. Dissipation is 60 mW @ 2 MHz. A single-chip CMOS/SOS CPU is in development.



Narrow 4-bit registers used to select 16-bit GP registers as pointers for full-range addressing. Must stop to preload, but 1-byte instructions possible.

HARDWARE SUPPORT: "Microkit" console ($2250) includes RAM, ROM, I/O decoders, teletype interface, power supply.

SOFTWARE:

Small, 59-command instruction set uses pointer-based architecture to achieve comparable performance to other NMOS μP's.

I—DATA MANIPULATION INSTRUCTIONS

Add, subtract and logical.
Reverse subtract (M - Accum).
Shift right one bit.
With immediate values.

II—DATA MOVEMENT INSTRUCTIONS

Addressing 2-stage using registers in 16×16 array as pointers. The 4-bit registers select pointers and define their function. The 4-bit register N designates the memory address register (MAR).
I/O and DMA control built into CPU.

III—PROGRAM MANIPULATION INSTR'S

Jump to subroutine by having 4-bit register "P" address different GP register in 16×16 array as PC. Return from subroutine by re-addressing original GP register as PC.
Can use pointers to create stacks in RAM.
Software maskable interrupt via line into CPU.

IV—PROGRAM STATUS MANIP. INSTR.

SOFTWARE SUPPORT: Assembly in Fortran IV on larger computers via TYMESHARE. Resident editor/assembler and debugging board optional for Microkit.