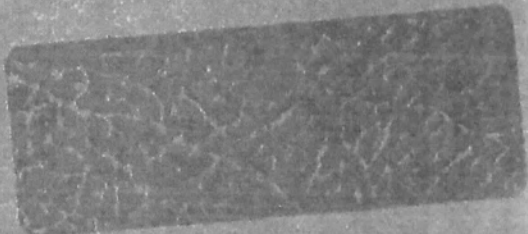


**8KRA STATIC READ/WRITE MEMORY
MODULE**

ASSEMBLY and TEST INSTRUCTIONS



Processor Technology Corporation
6200 Hollis Street
Emeryville CA 94608

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82928

8KRA STATIC READ/WRITE MEMORY
MODULE
ASSEMBLY and TEST INSTRUCTIONS

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SECTION I

INTRODUCTION AND GENERAL INFORMATION

8KRA STATIC READ/WRITE MEMORY MODULE
MANUAL



1.1 INTRODUCTION

This manual supplies the information needed to assemble, test and use the 8KRA Static Read/Write Memory Module. We suggest that you first scan the entire manual before starting assembly. Then make sure you have all the parts and components listed in the "Parts List" (Table 2-1) in Section II. When assembling the module, follow the instructions in the order given.

Should you encounter any problem during assembly, call on us for help if necessary. If your completed module does not work properly, recheck your assembly step by step. Most problems stem from poor soldering, backward installed components, and/or installing the wrong component. Once you are satisfied that the module is correctly assembled, feel free to ask for our help.

1.2 GENERAL INFORMATION

1.2.1 8KRA Memory Description

The 8KRA Static Read/Write Memory Module has a capacity of 8192 eight-bit bytes and operates in a static mode. As opposed to dynamic memories, the 8KRA needs only one power supply and does not require periodic refreshing.

All address and data lines are fully buffered, and extensive noise immunity circuitry is built into the memory. The module features switch selectable address selection which allows its starting address to be offset in 1K increments from zero to 65K.

Maximum worst case access time for the 8KRA is 520 nsec. Thus, in any 8080 system, this memory will operate at the same speed as any other memory with an access time between 50 and 520 nsec. Both the access time and non-refresh features of the 8KRA mean no computer "waiting" time is required.

The 8KRA Memory is plug-in compatible with the Altair 8800 bus. It requires +7.5 to +10 V dc at 1.9 amp (max.) operating power. In addition, the low power memory IC's used on the module can operate in a low power (+1.6 to 2.5 V dc at 0.9 amp max.) standby mode. Data loss from the 8KRA during loss-of-power or power interrupt conditions can consequently be prevented by using two "D" size batteries for standby power. Provisions for easily adding this standby capability are incorporated in the module design.

1.2.2 Receiving Inspection

When your module arrives, examine the shipping container for signs of possible damage to the contents during transit. Then inspect the contents for damage. (We suggest you save the shipping materials for use in returning the module to Processor Technology

should it become necessary to do so.) If your 8KRA kit is damaged, please write us at once describing the condition so that we can take appropriate action.

1.2.3 Warranty Information

In brief, the parts supplied with the module, as well as the assembled module, are warranted against defects in materials and workmanship for a period of 6 months after the date of purchase. Refer to Appendix I for the complete "Statement of Warranty".

1.2.4 Replacement Parts

Order replacement parts by component nomenclature (e.g., DM8131) and/or a complete description (e.g., 6.8 ohm, $\frac{1}{2}$ watt, 5% resistor).

1.2.5 Factory Service

In addition to in-warranty service, Processor Technology also provides factory repair service on out-of-warranty products. Before returning the module to Processor Technology, first obtain authorization to do so by writing us a letter describing the problem. After you receive our authorization to return the module, proceed as follows:

1. Write a description of the problem.
2. Pack the module with the description in a container suitable to the method of shipment.
3. Ship prepaid to Processor Technology, 6200 Hollis Street, Emeryville, CA 94608.

Your module will be repaired as soon as possible after receipt and return shipped to you prepaid.

SECTION II

ASSEMBLY

8KRA STATIC READ/WRITE MEMORY MODULE MANUAL



2.1 PARTS AND COMPONENTS

Check all parts and components against the "Parts List" (Table 2-1 on Page II-2). If you have difficulty in identifying any parts by sight, refer to Figure 2-1 on Page II-3.

2.2 ASSEMBLY TIPS

1. Scan Sections II and III in their entirety before you start to assemble your 8KRA Memory Module.

2. In assembling your 8KRA, you will be following a step-by-step assembly procedure. Follow the instructions in the order given.

3. Assembly steps and component installations are preceded by a set of parentheses. Check off each installation and step as you complete them. This will minimize the chances of omitting a step or a component.

4. When installing components, make use of the assembly aids that are incorporated on the 8KRA PC Board and the assembly drawing. (These aids are designed to assist you in correctly installing the components.)

a. The circuit reference (R3, C10 and IC20, for example) for each component is silk screened on the PC Board near the location of its installation.

b. Both the circuit reference and value or nomenclature (1.5K and 7400, for example) for each component are included on the assembly drawing near the location of its installation.

5. To simplify reading resistor values after installation, install resistors so that the color codes read from left-to-right and top-to-bottom as appropriate (board oriented as defined in Paragraph 2.5 on Page II-5).

6. Install disc capacitors as close to the board as possible.

7. Should you encounter any problem during assembly, call on us for help if needed.

2.3 ASSEMBLY PRECAUTIONS

2.3.1 Handling MOS Integrated Circuits

The memory IC's used in the 8KRA are MOS devices. They can be damaged by static electricity discharge. Always handle MOS IC's so that no discharge will flow through the IC. Also, avoid unneces-

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8KRA STATIC READ/WRITE MEMORY MODULE

SECTION II

Table 2-1. 8KRA Static Read/Write Memory Module Parts List.

<u>INTEGRATED CIRCUITS</u>	
1 74LS04 (IC79)	2 74LS283 (IC68 and 71)
1 74LS13 (IC72)	2 8T93 (IC77 and 78)
2 74LS132 (IC74 and 75)	2 8T98 or 8098 (IC69 and 76)
1 74LS136 (IC70)	64 91L02A or 21L02B (IC1 through 64)
1 74LS138 (IC67)	
<u>REGULATORS</u>	<u>DIODES</u>
2 340T-5.0 or 7805UC (IC65 and 66)	4 1N4001 or 1N4002 (D1 through D4)
	1 1N270 (D5)
<u>RESISTORS</u>	<u>CAPACITORS</u>
1 39 ohm, 2 watt, 5%	26 0.1 ufd, disc ceramic
2 470 ohm, $\frac{1}{4}$ watt, 5%	2 1 ufd, tantalum, dipped
11 1.5K ohm, $\frac{1}{4}$ watt, 5% or 2.2K ohm, $\frac{1}{4}$ watt, 5%	1 15 ufd, tantalum, dipped
<u>MISCELLANEOUS</u>	
1 8KRA PC Board	8 Augat Pins on Carrier
1 Heat Sink	1 Length #24 Bare Wire
1 6 or 7 Position DIP Switch	4 6-32 Screws
7 14-pin DIP Sockets	4 6-32 Lockwashers
70 16-pin DIP Sockets	4 6-32 Nuts
1 Right Angle Molex Connector, Male	1 Length Solder
1 Mating Connector for above, Female	1 Manual

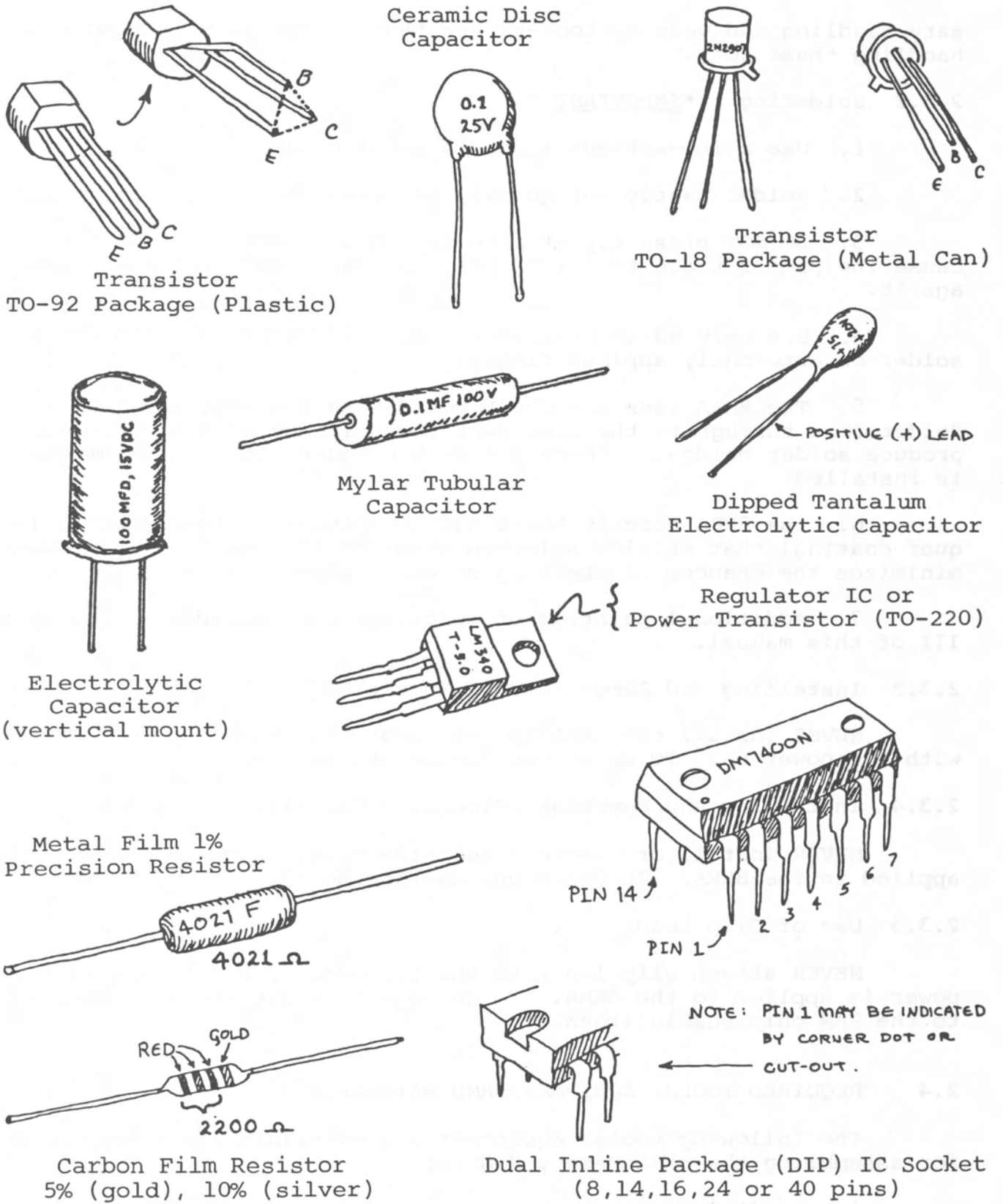


Figure 2-1. Identification of components.

sary handling and wear cotton--rather than synthetic--clothing when handling these IC's.

2.3.2 Soldering ****IMPORTANT****

1. Use a low-wattage iron, 25 watts maximum.
2. Solder neatly and quickly as possible.
3. DO NOT press tip of iron on pad or trace. To do so can cause the pad or trace to "lift" off the board and permanently damage it.
4. Use only 60-40 rosin-core solder. NEVER use acid-core solder or externally applied fluxes.
5. The 8KRA uses a circuit board with plated-through holes. Solder flow through to the component (front) side of the board can produce solder bridges. Check for such bridges after each component is installed.
6. The 8KRA circuit board has an integral solder mask (a lacquer coating) that shields selected areas on the board. This mask minimizes the chances of creating solder bridges during assembly.
7. Additional pointers on soldering are provided in Appendix III of this manual.

2.3.3 Installing and Removing 8KRA Module

NEVER install the 8KRA in, or remove it from, the computer with the power on. To do so can damage the module.

2.3.4 Installing and Removing Integrated Circuits

NEVER install or remove integrated circuits while power is applied to the 8KRA. To do so can damage the IC.

2.3.5 Use of Clip Leads

NEVER attach clip leads to the top edge of the module when power is applied to the 8KRA. To do so will short the +8 V dc bus to the RAM chip enable lines.

2.4 REQUIRED TOOLS, EQUIPMENT AND MATERIALS

The following tools, equipment and materials are recommended for assembling the 8KRA Memory Module:

1. Needle nose pliers

2. Diagonal cutters.
3. Controlled heat soldering iron, 25 watts
4. 60-40 rosin-core solder (supplied)
5. Volt-ohmmeter

2.5 ORIENTATION

The heat sink area (large foil area) will be located in the upper righthand corner of the board when the edge connector is positioned at the bottom of the board. In this position, the component (front) side of the board is facing up. Subsequent position references assume this orientation.

2.6 ASSEMBLY PROCEDURE

Refer to the assembly drawing in Section V.

CAUTION

THIS DEVICE USES MOS MEMORY INTEGRATED CIRCUITS (IC1 - 64) WHICH CAN BE DAMAGED BY STATIC ELECTRICITY DISCHARGES. HANDLE THESE IC'S SO THAT NO DISCHARGE FLOWS THROUGH THE IC. AVOID UNNECESSARY HANDLING AND WEAR COTTON CLOTHING -- RATHER THAN SYNTHETIC CLOTHING -- WHEN HANDLING THESE IC'S. (STATIC CHARGE PROBLEMS ARE MUCH WORSE IN LOW HUMIDITY ENVIRONMENTS.)

() Step 1. Check circuit board to insure that there are no shorts between the memory chip mounting pads and that neither the +8-volt bus nor the +5-volt bus are shorted to ground. Using an ohmmeter on its lowest scale, make the following measurements:

() 8-volt Bus Test. Measure between edge connector pin 1 or 51 (left end of connector) and pin 50 or 100 (right end of connector). There should be no continuity.

() 5-volt Bus Test. Measure between positive mounting pad for C23 and pin 50 or 100 of edge connector. Also measure between positive mounting pad for C22 and pin 50 or 100 of edge connector. There should be no continuity in either measurement.

() RAM Area Test. Measure between ground (edge connector pin 50 or 100) and each mounting pad (excluding pad 9

which is connected to ground) for IC1. Also measure between +5-volt bus (positive mounting pad for C23) and each mounting pad (excluding pad 10 which is connected to +5 volts) for IC1. Then measure between all combinations of vertically and horizontally adjacent pads for IC1. There should be no continuity in any of these measurements.

If you measure continuity in any of the preceding tests, the PC Board is defective and should be returned to Processor Technology for replacement. If none of the measurements show continuity, proceed to Step 2.

✓ Step 2. Install heat sink. Position the large, black heat sink (flat side to board) over the square foil area in the upper right corner. Orient the sink so that the two triangles of mounting holes in the board are under the triangular cut-outs in the sink. Using two 6-32 screws, lockwashers and nuts, attach heat sink to board. Insert screws from back (solder) side of board. (See Figure 2-2.)

✓ Step 3. Install IC65 and IC66 (340T-5.0 or 7805UC). Position IC65 on the heat sink and observe how leads must be bent to fit the mounting holes. Note that the center lead (3) must be bent down at a point approximately 0.2 inches further from the body than the other leads. Bend leads so no contact is made with heat sink when IC65 is flat against the sink and its mounting hole is aligned with the hole in the sink. Fasten IC65 to sink using 6-32 screw, lockwasher and nut. Insert screw from back (solder) side of board. Solder and trim leads. Install IC66 the same way as you did IC65. (See Figure 2-2.)

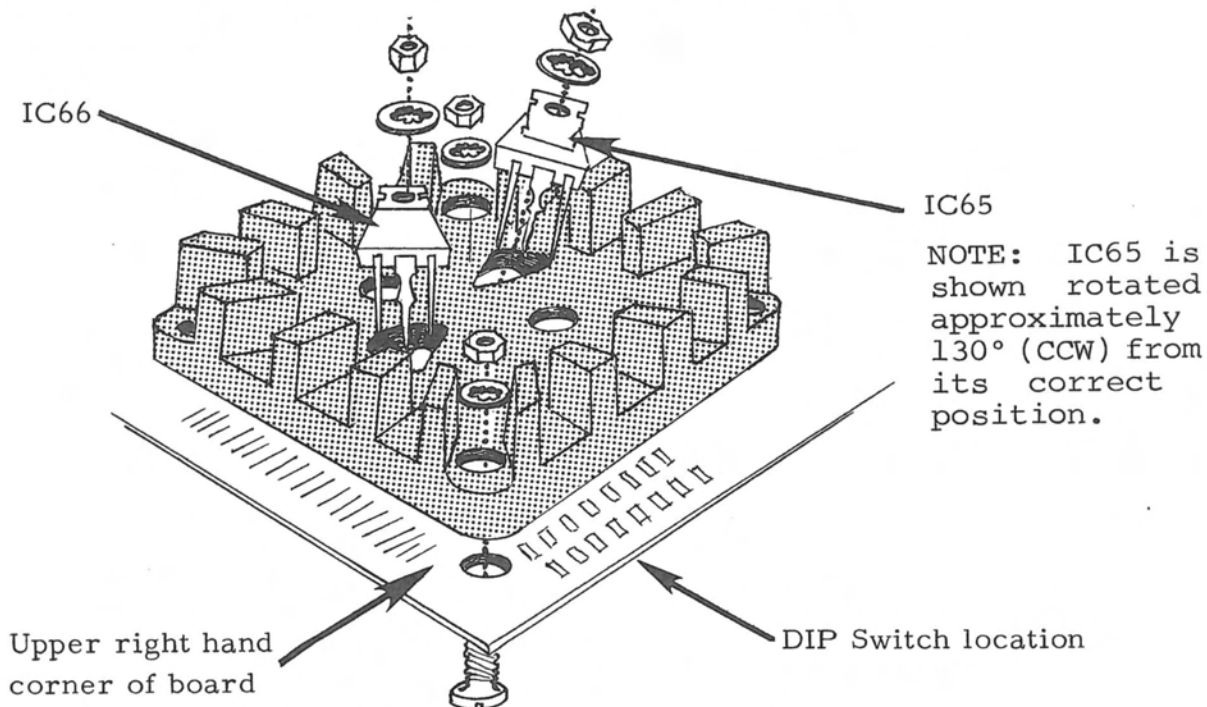


Figure 2-2. Heat sink and IC65 and IC66 installation.

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- (✓) Step 4. Install male Molex right angle connector in its location directly above the heat sink. Position connector with the longer pins at the top, insert leads in mounting holes, solder and trim leads.
- (✓) Step 5. Install diode D5 (1N270) in its location to the right of Area B. Position D5 so that its dark band mark (cathode) is on the righthand side. Solder and trim leads.
- (✓) Step 6. Install diodes D1, D2, D3 and D4 (1N4001 or 1N4002) in their locations above the heat sink. Position D1, D3 and D4 so that their dark band marks (cathode) are at the bottom, and position D2 so that its dark band is at the top.
- (✓) Step 7. Install the three tantalum capacitors in the following locations. Take care to observe proper values and the correct orientation.

<u>LOCATION</u>	<u>VALUE (ufd)</u>	<u>ORIENTATION</u>
(✓) C21	15	"+" lead top
(✓) C22	1	"+" lead bottom
(✓) C23	1	"+" lead right

Check the capacitors for correct value and orientation, bend leads outward on solder (back) side of board, solder and trim.

- (✓) Step 8. Install disc capacitors in numerical order in the indicated locations. Insert leads, pull down snug to board, bend leads outward on solder (back) side of board, solder and trim.

NOTE

Disc capacitor leads are usually coated with wax during the manufacturing process. After inserting leads through mounting holes, remove capacitor and clear the holes of any wax. Reinsert and install.

<u>LOCATION</u>	<u>VALUE (ufd)</u>	<u>TYPE</u>
(✓) C1	0.1	Disc Ceramic
(✓) C2	0.1	Disc Ceramic
(✓) C3	0.1	Disc Ceramic
(✓) C4	0.1	Disc Ceramic
(✓) C5	0.1	Disc Ceramic
(✓) C6	0.1	Disc Ceramic
(✓) C7	0.1	Disc Ceramic
(✓) C8	0.1	Disc Ceramic

(Continued on Page II-8.)

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() Step 8. (continued)

<u>LOCATION</u>	<u>VALUE (ufd)</u>	<u>TYPE</u>
C9	0.1	Disc Ceramic
C10	0.1	Disc Ceramic
C11	0.1	Disc Ceramic
C12	0.1	Disc Ceramic
C13	0.1	Disc Ceramic
C14	0.1	Disc Ceramic
C15	0.1	Disc Ceramic
C16	0.1	Disc Ceramic
C17	0.1	Disc Ceramic
C18	0.1	Disc Ceramic
C19	0.1	Disc Ceramic
C20	0.1	Disc Ceramic
C24	0.1	Disc Ceramic
C25	0.1	Disc Ceramic
C26	0.1	Disc Ceramic
C27	0.1	Disc Ceramic
C28	0.1	Disc Ceramic
C29	0.1	Disc Ceramic

() Step 9. Install all resistors in numerical order in the indicated locations. Bend leads to fit distance between the mounting holes, insert leads, pull down snug to board, bend leads outward on back (solder) side of board, solder and trim. Refer to footnote at the end of this step before installing asterisked (*) resistor.

<u>LOCATION</u>	<u>VALUE (ohms)</u>	<u>COLOR CODE</u>
() R1*	39, 2 watt	orange-white-black
R2	1.5K (or 2.2K)	brown-green-red**
R3	1.5K (or 2.2K)	brown-green-red**
R4	1.5K (or 2.2K)	brown-green-red**
R5	1.5K (or 2.2K)	brown-green-red**
R6	1.5K (or 2.2K)	brown-green-red**
R7	1.5K (or 2.2K)	brown-green-red**
R8	1.5K (or 2.2K)	brown-green-red**
R9	1.5K (or 2.2K)	brown-green-red**
R10	1.5K (or 2.2K)	brown-green-red**
R11	470	yellow-violet-brown
R12	1.5K (or 2.2K)	brown-green-red**
R13	470	yellow-violet-brown
R14	470	yellow-violet-brown

*DO NOT install R1 unless battery standby power is to be used.

**red-red-red if 2.2K ohms

- () Step 10. Install Augat pins as follows:

NOTE

You will find it helpful to hold the board between two objects so that it stands on one edge.

- (/) Area C. Remove two pins from one-half of the carrier. Insert them into the mounting holes from front (component) side of board. Solder pins from back (solder) side of the board so that the solder "wicks up" to the front side. (This will hold the pins firmly in place.)

Insert a component lead into one pin and reheat the solder. Using the component lead, adjust pin until it is perpendicular to board. Allow solder to cool while holding the pin as steady as possible. Repeat with other pin.

NOTE

If the cooled solder is mottled or crystallized, a "cold joint" is indicated, and the solder should be reheated.

Check both installations for cold joints and solder bridges.

- (/) Area B. Remove three more pins from the carrier and install them in mounting holes P, CLR and U. Install these as you did the Area C pins. Check for cold joints and solder bridges.

- (/) Area A. Remove remaining three pins from carrier. Install two of them in mounting holes W and Ø. Install the third in mounting holes 1 or 2 if desired (refer to Section III of this manual). Install these pins as you did the Area C pins. Check for cold joints and solder bridges.

NOTE

Only three Augat pins are supplied for Area A since the 8KRA runs at maximum speed and requires no wait states. Should you have a pin available and wish to install it in the remaining mounting hole, do so.

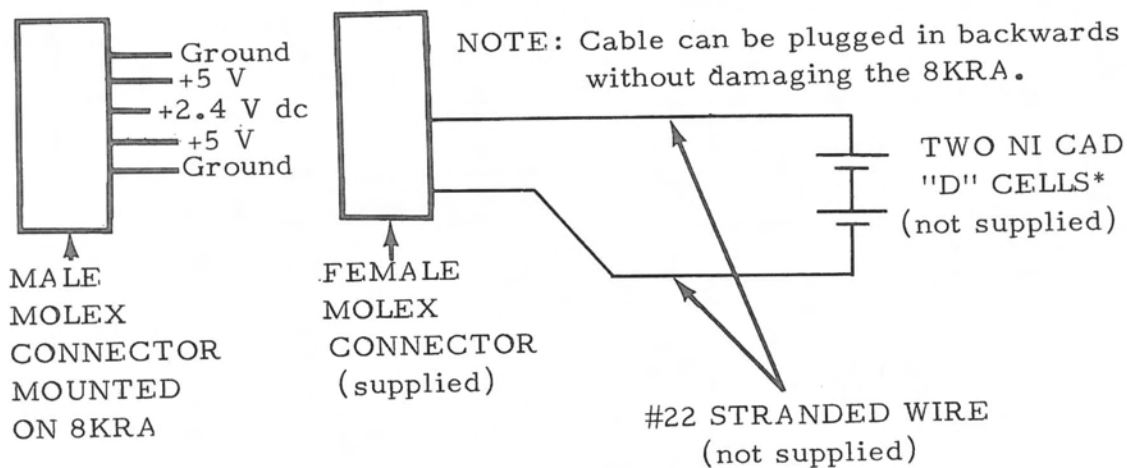
- (/) Step 11. Install DIP Switch in its location in the upper right corner above the heat sink. Position it so Switch No. 1 is at the left. As you will note, the DIP Switch

mounting area is designed to accommodate a 7-position switch. If a 6-position switch (12 pins) is supplied, position it as far to the left as possible. (The two holes to the right will be unused in this case.) If a 7-position switch (14 pins) is supplied, remember that Switch No. 7 is not used.

✓) Step 12. Fill all exposed (not covered with lacquer) feed-through holes to the right of IC16, IC32, IC48 and IC64.

✓) Step 13. Using the #24 bare wire, install jumpers in Areas A, B and C according to your selection of the options that are described in Section III of this manual.

() Step 14. If you intend to use the battery standby power feature of the 8KRA, fabricate a "cable" to interconnect the 8KRA and your standby supply. A mating connector for the male Molex you installed in Step 4 is provided for this purpose. Fabrication and power supply details are shown in Figure 2-3.



*Standard or alkaline batteries, with their attendant shorter life, may also be used. Recharging circuitry on the 8KRA continuously charges batteries during normal operation.

Figure 2-3. Standby power supply and interconnection.

- (✓) Step 15. Install RAM DIP sockets and check installations. Install these sockets in the indicated locations with their end notches oriented as shown on the assembly drawing. Take care not to create solder bridges between the pins and/or traces. (Note that after each row of sockets--e.g., IC1 through IC16 and IC17 through IC32--is installed, you will be testing for shorts.)
- (✓) IC1 through IC16. Install 16-pin DIP sockets in locations IC1 through IC16. Then perform the "RAM Area Test" described in Step 1 of the Assembly Procedure. Make the measurements at IC1. If any of the tests fail, you created a solder short at one or more points in the row of sockets just installed. Find and eliminate the short(s) before proceeding further. If your installations pass the test, continue on to the next row.
- (✓) IC17 through IC32. Install 16-pin DIP sockets in locations IC17 through IC32. Check this row as you did IC1 through IC16, but make the measurements at IC17.
- (✓) IC33 through IC48. Install 16-pin DIP sockets in locations IC33 through IC48. Check this row as you did IC1 through IC16, but make the measurements at IC33.
- (✓) IC49 through IC64. Install 16-pin DIP sockets in locations IC49 through IC64. Check this row as you did IC1 through IC16, but make the measurements at IC49.

After installing the sockets for IC1 through IC64 and checking your installations for freedom from shorts, proceed to the next step.

- (✓) Step 16. Install remaining DIP sockets. Install each socket in the indicated location with its end notch oriented as shown on the assembly drawing. Take care not to create solder shorts between the pins and/or traces.

<u>LOCATION</u>	<u>SOCKET TYPE</u>
(✓) IC70	14 pin
(✓) IC72	14 pin
(✓) IC74	14 pin
(✓) IC75	14 pin
(✓) IC77	14 pin
(✓) IC78	14 pin
(✓) IC79	14 pin
(✓) IC67 through IC69	16 pin
(✓) IC71	16 pin
(✓) IC73	16 pin
(✓) IC76	16 pin

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() Step 17. Check regulator operation. This check is made to prevent potential subsequent damage to the IC's from incorrect voltages.

(/) Install 8KRA in computer. (The use of a Processor Technology EXB Extender Board is recommended.)

CAUTION

NEVER INSTALL OR REMOVE CIRCUIT BOARD WITH POWER ON. TO DO SO CAN DAMAGE THE BOARD.

(/) Turn power on and measure the voltage between ground and each of the +5 V pins of the Molex connector (see Figure 2-3 on Page II-10). You should measure +5 V dc \pm 5% in each case.

(/) If either voltage is incorrect, determine and correct the cause before proceeding. Especially check for solder shorts.

(/) If voltages are correct, turn power off, remove module from computer, and go on to Step 18.

(/) Step 18. Install the following IC's in the indicated locations. Pay careful attention to the proper orientation.

NOTE

Pin 1 is indicated by a dot on the PC Board and assembly drawing.

<u>IC NO.</u>	<u>TYPE</u>
(/) IC67	74LS138
(/) IC68	74LS283
(/) IC69	8T98 or 8098
(/) IC70	74LS136
(/) IC71	74LS283
(/) IC72	74LS13
NA (/) IC73*	74LS109 (not supplied)
(/) IC74	74LS132
(/) IC75	74LS132
(/) IC76	8T98 or 8098
(/) IC77	8T93
(/) IC78	8T93
(/) IC79	74LS04

*This IC, the "wait state counter", is not required since the 8KRA runs at maximum speed. IC73 is consequently not supplied with your kit. For special applications, a 74LS109 can be used in this location.

- (X) Step 19. Install IC1 through IC64 in numerical order in their respective locations. Pay careful attention to the proper orientation.

IC1 through IC64 (type 91L02A or 21L02B) are MOS devices. Refer to the CAUTION on Page II-5.

- (X) Step 20. Install the 8KRA in your computer and test it for proper operation. Test programs and instructions for testing the module are provided in Appendix VI of this manual.

CAUTION

NEVER INSTALL OR REMOVE 8KRA WITH COMPUTER POWER ON.

SECTION III

OPTION SELECTION

8KRA STATIC READ/WRITE MEMORY MODULE MANUAL



3.1 OPTION SELECTION

Jumper options that control three operating parameters are provided on the 8KRA Memory Module. They are: phantom memory disable, power-up initialization, and waiting time. The starting address is switch selectable. Use the following option selection instructions in conjunction with the assembly drawing in Section V.

3.2 WAITING TIME OPTION (AREA A)

Since the 8KRA operates at maximum speed, you normally will not enable the waiting time option.

To configure the 8KRA for no waiting time, install a jumper (#24 bare wire is recommended) between the W and \emptyset pins in Area A.

For special applications, you may wish to enable the waiting time option. You have, in this case, a choice of enabling one or two wait states. Each state is 0.5 usec in duration.

NOTE

Wait states cannot be selected unless IC73, the "wait state counter", is installed.

To select one wait state, install a jumper (#24 bare wire is recommended) between the W and 1 pins in Area A.

To select two wait states, install a jumper (#24 bare wire is recommended) between the W and 2 pins in Area A.

3.3 POWER-UP INITIALIZATION OPTION (AREA B)

The jumper arrangement in Area B determines whether the 8KRA will come up in the protected or unprotected mode when power is initially applied or restored after a power failure. In the protect mode, a random operation cannot improperly rewrite retained data.

To select the power-up protect mode, install a jumper (#24 bare wire is recommended) between the CLR and P pins in Area B.

To select the power-up unprotect mode, install a jumper (#24 bare wire is recommended) between the CLR and U pins in Area B.

3.4 MEMORY DISABLE OPTION (AREA C)

Select the phantom disable option only if the 8KRA is to be used at address zero with a Processor Technology ALS-8 Firmware Module. Selection is accomplished by installing a jumper (#24 bare wire is recommended) between the two Augat pins in Area C. With this jumper installed, the 8KRA will be disabled by the signal, PHANTOM, which is supplied by the ALS-8 on Bus Pin 67.

If the 8KRA is not to be used at address zero with the ALS-8, DO NOT install a jumper in Area C.

3.5 STARTING ADDRESS SELECTION

One of 64 possible starting addresses for the 8KRA is selected with the six DIP switch positions in the upper right corner of the module.

To select the desired address, set the DIP switches as shown in Table 3-1.

Table 3-1. 8KRA Starting Address Selection.

STARTING ADDRESS*		DIP SWITCH SETTINGS					
		Address			Offset		
Decimal	Hex	A15	A14	A13	A12	A11	A10
0	0000	-	-	-	-	-	-
1,024	0400	-	-	-	-	-	C
2,048	0800	-	-	-	-	C	-
3,072	0C00	-	-	-	-	C	C
4,096	1000	-	-	-	C	-	-
5,120	1400	-	-	-	C	-	C
6,144	1800	-	-	-	C	C	-
7,168	1C00	-	-	-	C	C	C
8,192	2000	-	-	C	-	-	-
9,216	2400	-	-	C	-	-	C
10,240	2800	-	-	C	-	C	-
11,264	2C00	-	-	C	-	C	C
12,288	3000	-	-	C	C	-	-
13,312	3400	-	-	C	C	-	C
14,336	3800	-	-	C	C	C	-
15,360	3C00	-	-	C	C	C	C
16,384	4000	-	C	-	-	-	-
17,408	4400	-	C	-	-	-	C
18,432	4800	-	C	-	-	C	-
19,456	4C00	-	C	-	-	C	C
20,480	5000	-	C	-	C	-	-
21,504	5400	-	C	-	C	-	C
22,528	5800	-	C	-	C	C	-
23,552	5C00	-	C	-	C	C	C
24,576	6000	-	C	C	-	-	-
25,600	6400	-	C	C	-	-	C
26,624	6800	-	C	C	-	C	-
27,648	6C00	-	C	C	-	C	C

8KRA STATIC READ/WRITE MEMORY MODULE

SECTION III

Decimal	Hex	A15	A14	A13	A12	A11	A10
28,672	7000	-	C	C	C	-	-
29,696	7400	-	C	C	C	-	-
30,720	7800	-	C	C	C	C	-
31,744	7C00	-	C	C	C	C	C
32,768	8000	C	-	-	-	-	-
33,792	8400	C	-	-	-	-	C
34,816	8800	C	-	-	-	C	-
35,840	8C00	C	-	-	-	C	C
36,864	9000	C	-	-	C	C	-
37,888	9400	C	-	-	C	-	-
38,912	9800	C	-	-	C	C	C
39,936	9C00	C	-	-	C	C	C
40,960	A000	C	-	C	-	-	-
41,984	A400	C	-	C	-	-	-
43,008	A800	C	-	C	-	C	-
44,032	AC00	C	-	C	-	C	C
45,056	B000	C	-	C	C	-	-
46,080	B400	C	-	C	C	-	C
47,104	B800	C	-	C	C	C	-
48,128	BC00	C	-	C	C	C	C
49,152	C000	C	C	-	-	-	-
50,176	C400	C	C	-	-	-	C
51,200	C800	C	C	-	-	C	-
52,224	CC00	C	C	-	-	C	C
53,248	D000	C	C	-	C	-	-
54,272	D400	C	C	-	C	-	C
55,296	D800	C	C	-	C	C	-
56,320	DC00	C	C	-	C	C	C
57,344	E000	C	C	C	-	-	-
58,368	E400	C	C	C	-	-	C
59,392	E800	C	C	C	-	C	-
60,416	EC00	C	C	C	-	C	C
61,440	F000	C	C	C	C	-	-
62,464	F400	C	C	C	C	-	C
63,488	F800	C	C	C	C	C	-
64,512	FC00	C	C	C	C	C	C

- = switch is off or open
 C = switch is on or closed

* Only the indicated starting addresses are available.
 No intermediate addresses can be used.

SECTION V

DRAWINGS

8KRA STATIC READ/WRITE MEMORY MODULE

See
page

33 - 36 below



SECTION IV

THEORY OF OPERATION

8KRA STATIC READ/WRITE MEMORY MODULE
MANUAL



4.1 GENERAL DESCRIPTION

Refer to the 8KRA schematic in Section V of this manual.

Address lines A \emptyset through A9 are buffered from the bus through IC77 and IC78 to the ten address input pins on each RAM (random access memory) chip, IC1 through IC64. The memory matrix consists of eight, 1024-word "pages". Only one page at a time, however, is selected to read information to, or write information from, the data buses.

In a memory write operation, the 8KRA writes data from the data-out bus, DO \emptyset through DO7. Each data-out line is buffered (IC78 and IC79) to the DI (data-in) input of one RAM chip in each page of memory. Thus, each RAM chip in a page stores one bit of the word in that page.

In the memory read mode, the 8KRA reads information to the data-in bus, DI \emptyset through DI7. The DO (data-out) outputs of the RAM chips are tri-state types that float in a high-impedance state when they are not selected. They can therefore be--and are--connected in parallel from one page to the next. As a result, only the bits in the selected page can be gated by IC69 and IC76 to DI \emptyset through DI7.

Full addressing of the 8KRA is done on A \emptyset through A15, with each of the following segments performing the indicated function:

<u>ADDRESS BITS</u>	<u>FUNCTION</u>
A \emptyset - A4	Selects row inside RAM chips (one of 32)
A5 - A9	Selects column inside RAM chips (One of 32)
A1 \emptyset - A12	Selects memory page (one of eight)
A13 - A15	Selects 8KRA module (one of eight)

4.2 READ OPERATION

Data from the selected memory page is applied to tri-state bus drivers, IC69 and IC76. The drivers are enabled only if the output on pin 6 of IC72 is low. This only occurs when all four inputs are high.

Pin 6 of IC72 is low when: 1) SMEMR and PDBIN are high and 2) the wire OR'ed output of comparator IC70 (pins 3, 6, 8 and 11) is high. The first condition occurs when the data bus is to be used for memory read data and the data bus is in the input mode. The second condition occurs when the 8KRA is specifically addressed and SOUT and SINP are low.

IC68 and IC71 are 4-bit binary adders/subtractors. IC68 adds the complement (set by the Offset Switches) of the A1 \emptyset through

A12 bits in the module address to the actual corresponding bus address bits in order to provide the page selection inputs (A, B, C) for IC67, a 3-to-8 line decoder. The fourth section in IC68 adds any carry from the A12 addition and the A13 bus address bit to provide the input on pin 1 of IC70. The first two sections of IC71 add "1" to the A14 and A15 bits in the module address and supply the sums to pins 4 and 10 of IC70.

Since the Address Switches reflect the complement of the three most significant bits in the module address, the three corresponding outputs of IC68 and IC71 will reflect the A13 through A15 bits in the module address if, and only if, that address is presented on the address lines. When this is the case, pins 3, 6 and 8 of IC70 are high, as will be the output on pin 13 of IC71. (Pin 13 of IC71 is low only if an address not within the selected range for the module appears on the address lines.) Pin 11 of IC70 will also be high for a read (or write) operation. (Note that the fourth section in IC70 is used only to invert SOUT.)

Pin 6 of IC72 and pin 8 of IC75 are now low by virtue of SMEMR and PDBIN being high, pin 10 of IC71 is high, and the wire OR'ed output of IC70 is high. The low on pin 6 of IC72 enables the data-in bus (DI0 through DI7) drivers, IC69 and IC76. The low on pin 8 of IC75 provides the second enable required by IC67 to decode its inputs and enable the eight RAM's in the selected page.

If the 8KRA is used at address zero with a Processor Technology ALS-8 Firmware Module, the Area C jumper will be in. When the ALS-8 generates PHANTOM, the B2 (pin 2) input to IC71 goes low. The output on pin 13 will be low for all combinations of A14 and A15. Pins 8 and 6 of IC72 and pin 8 of IC75 will thus all be high to disable \overline{WE} , IC67 and the data input bus drivers, IC69 and IC76. That is, the 8KRA is disabled.

4.3 WRITE OPERATION

A write operation is similar to the read operation except MWRT is high instead of SMEMR. IC69 and IC76 are disabled and pin 13 of IC69 is low for the duration of the MWRT pulse. The CPU controls the timing of this pulse. With pin 13 of IC69 low, all RAM's are partially enabled to read data from the DO bus. The page to be written into is selected by A10 and A11.

In order for pin 13 of IC69 to be low, pin 6 of IC75 must be high and the module must be selected (all outputs of IC70 and the Z3 output of IC71 are high). Three gates in IC75 and one in IC74 are connected as a latch which is set or reset by the PROT and UNPROT signals on Bus Pins 70 and 20. When PROT goes high to set the latch, pin 3 of IC75 goes high and pin 6 of IC75 goes low. This low inhibits \overline{WE} and provides an active low \overline{PS} signal on pin 13 of IC76. A low \overline{PS} turns the computer PROT light on to indicate that the page of

memory is protected. When UNPROT goes high, the latch resets so that pin 6 of IC75 is high to enable memory write operations on the module.

The jumper arrangement in Area B is used to select the power-up protect or power-up unprotect mode. In brief, Area B permits POC to perform the same function as PROT (CLR-to-P jumpered) or UNPROT (CLR-to-U jumpered) when computer power is turned on. If neither jumper is installed, it is necessary to issue the proper PROT or UNPROT signals to memory when first powering the computer in order to guarantee a known state.

4.4 WAIT STATES

The RAM chips supplied with the 8KRA provide valid data within one CPU cycle time (500 nsec). When such fast RAM's are used, the Area A jumper which selects waiting time is connected to the \emptyset terminal. This connects a "low" level to pin 12 of IC76. When this section of the bus driver is enabled (a low on pin 15) by a low on pin 8 of IC75, the PRDY signal to the bus is driven high. Therefore, the 8KRA sends a "ready" signal back as soon as it is addressed. The data will be ready before the processor is.

In certain special applications, or if slower RAM chips or a faster CPU are used, one or two "wait" cycles must be allowed to pass before the CPU is allowed to accept data. IC73 comprises a two-bit shift register which may be selected to give a low level at pin 7 or pin 9 after one or two $\emptyset 2$ pulses. IC73 is a dual J-K flip-flop with positive clock. The outputs of each section change on the low-to-high transition of the clock signal, depending on the condition of the J and \bar{K} inputs. The changes occur according to the following table:

J high, \bar{K} high	Q goes high
J low, \bar{K} low	Q goes low

When PSYNC goes high, both sections in IC73 are reset (pin 6 goes low; pins 7 and 9 go high). When PSYNC goes low, section 1 may change state on the next high-to-low transition of $\emptyset 2$ clock. (Note that section 2 will not change state on the next transition since its J and \bar{K} inputs are both low.)

On the first $\emptyset 2$ transition after PSYNC goes low, pins 6 and 7 will go high and low respectively. Section 2, with its J and \bar{K} inputs both high, will consequently change state on the second High-to-low $\emptyset 2$ transition after PSYNC goes low. As a result, pin 9 goes low. (Section 1 cannot change state on this transition since its J and \bar{K} inputs are both high.)

Now both sections are set, and they will remain so until PSYNC resets them. If IC73 and the W-to-1 jumper are installed,

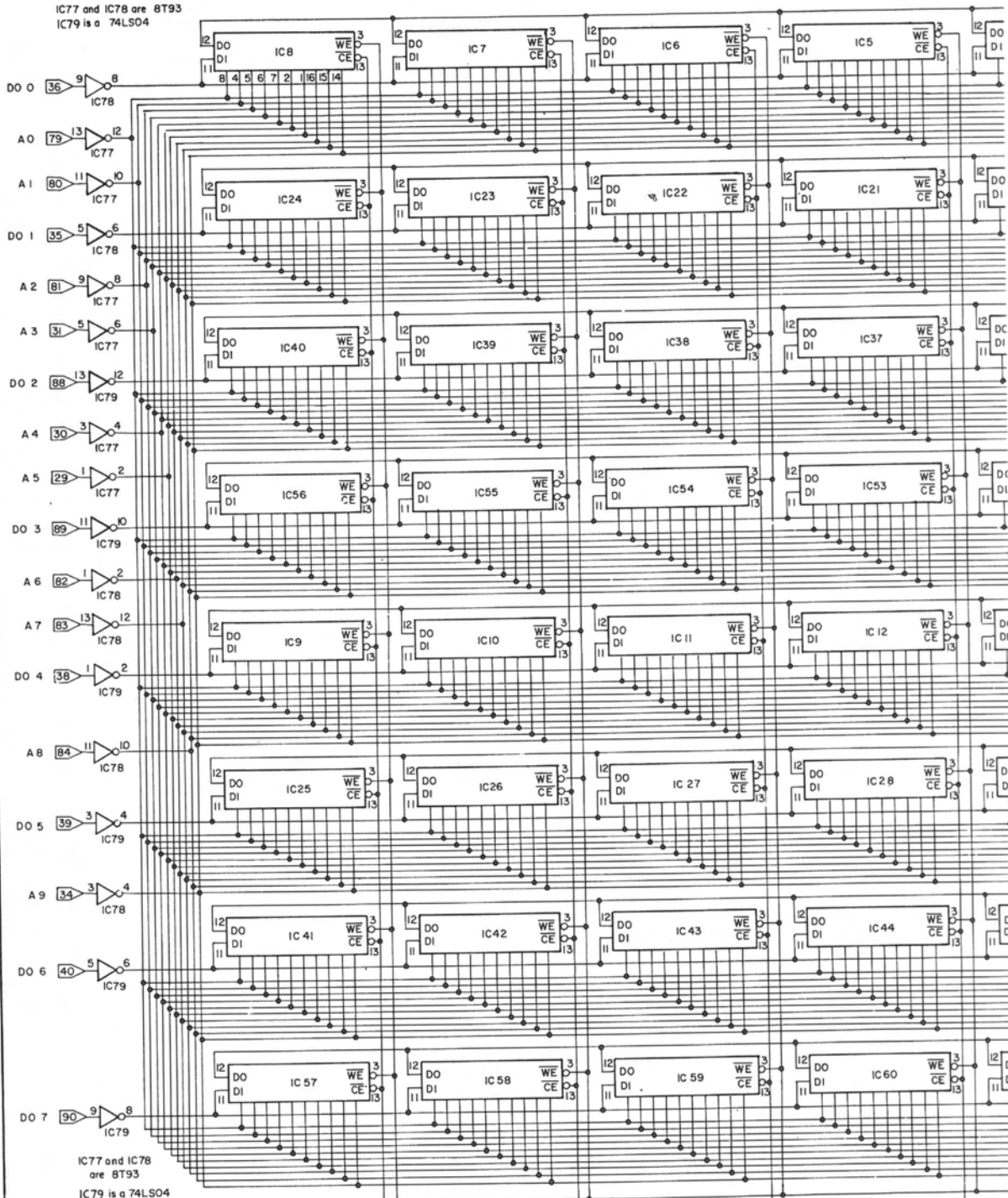
pin 23 of IC76 will go low on the first high-to-low transition of ϕ_2 after PSYNC. With two wait states selected (W-to-2 jumper in), pin 12 of IC76 will go low after the second high-to-low transition of ϕ_2 after PSYNC. Inversion in IC76 drives the PRDY bus line high in either case to send a "ready" signal to the processor.

4.5 POWER SUPPLY

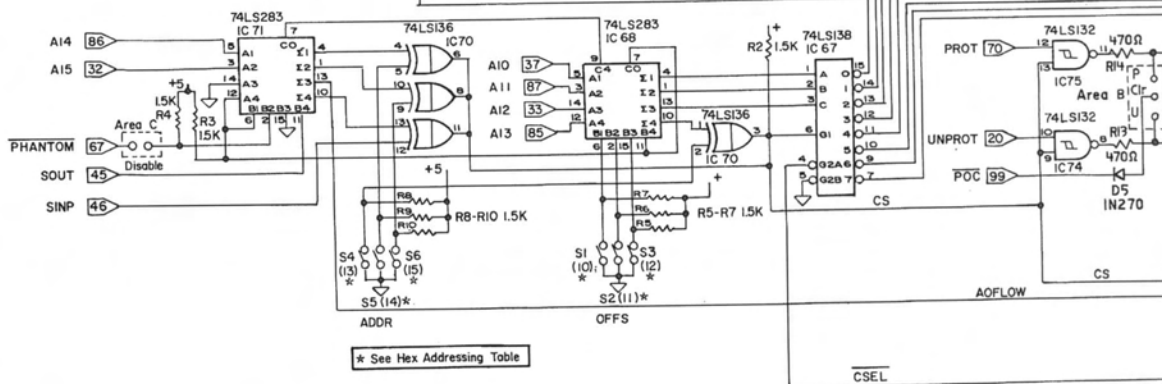
IC76 and IC66 are series voltage regulators that supply on-card regulation to maintain the constant 5 V dc outputs. Input bypass capacitor (C21) provides additional filtering of the 8 V dc input, and the output bypass capacitors (C22 and C23) improve transient response by attenuating transients.

Diode D2 is a protective shunt that prevents damage to the 8KRA if it is plugged into the computer backwards. D1 and limiting resistor R1 permit the standby battery supply (if used) to continuously charge during normal operation. Should there be a power loss, and the standby power supply is connected, D3 and D4 conduct to make battery power available to the 8KRA. Under normal operating conditions, D3 and D4 isolate the standby supply from +5 V dc.

IC77 and IC78 are 8T93
IC79 is a 74LS04

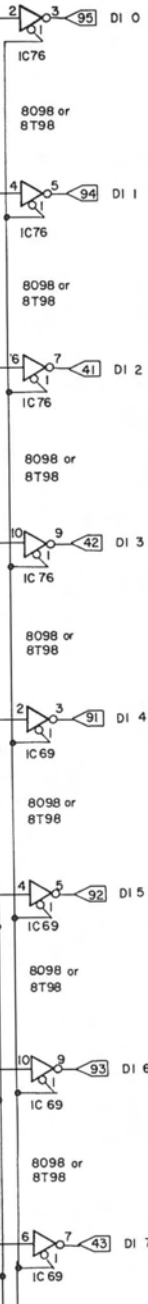
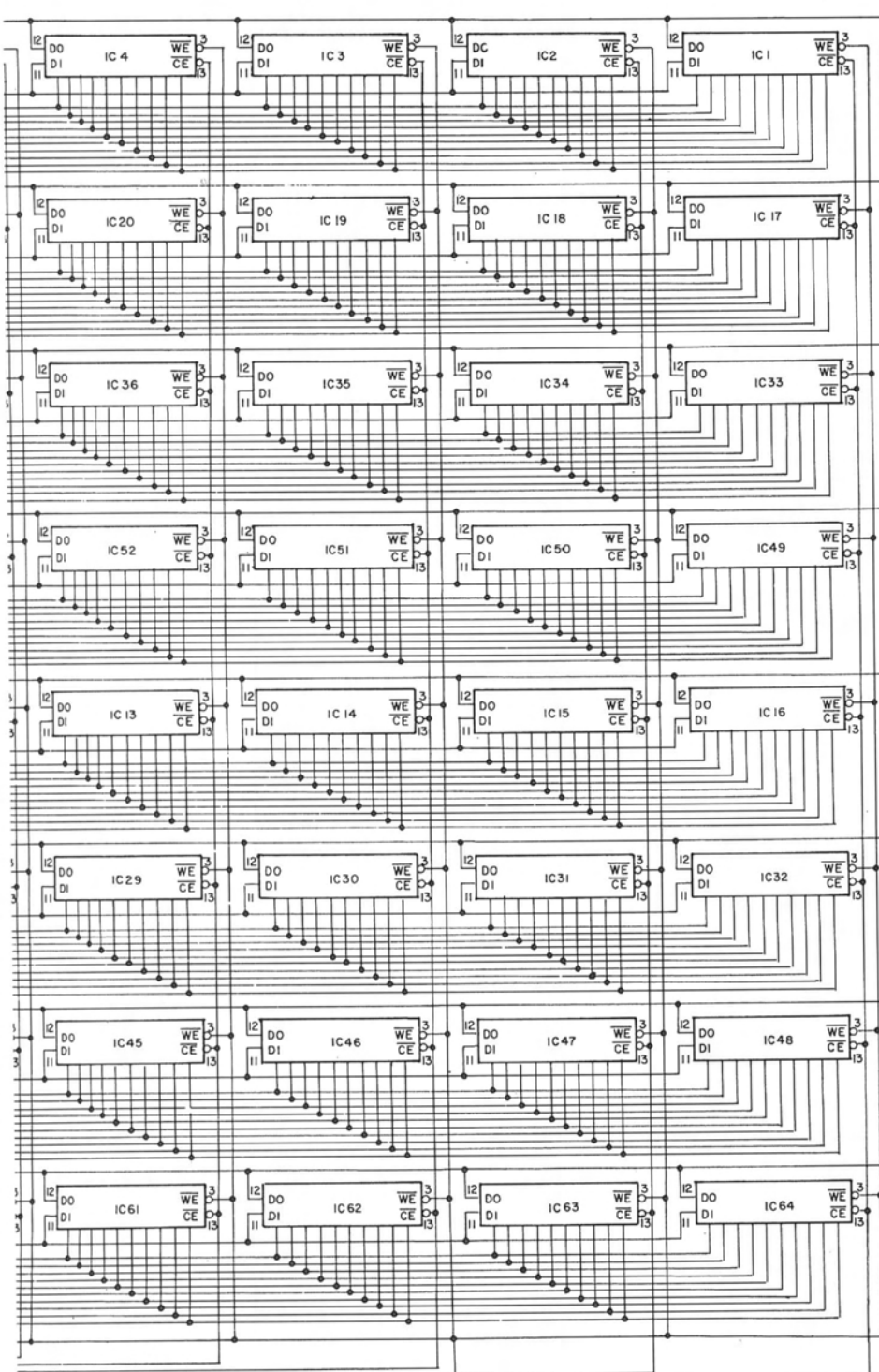


IC77 and IC78
are 8T93
IC79 is a 74LS04



* See Hex Addressing Table

CSEL

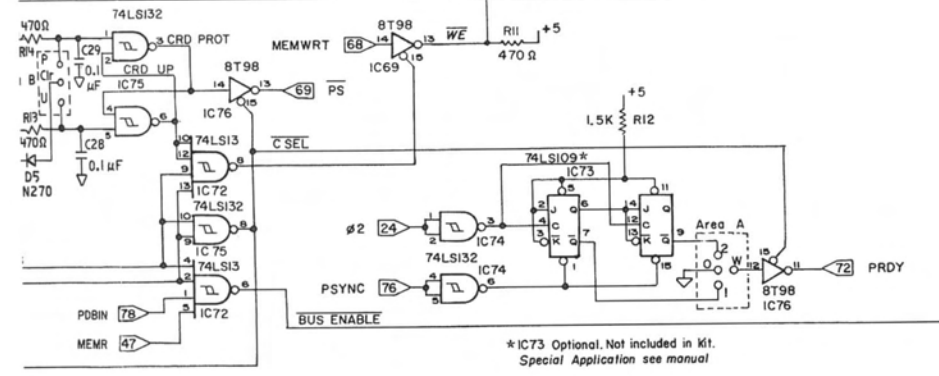


Hex Addressing Table

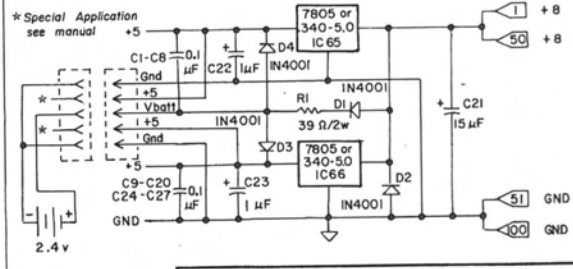
Address Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	OFFS
0 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	000
0 0 1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1000
0 1 0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	2000
0 1 1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	2400
1 0 0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	4000
1 0 1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	4400
1 1 0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	6000
1 1 1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	6400
0 0 0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8000
0 0 1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8400
0 1 0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1000
0 1 1	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	10400
1 0 0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12000
1 0 1	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	12400
1 1 0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	14000
1 1 1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	14400
0 0 0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16000
0 0 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	16400
0 1 0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	18000
0 1 1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	18400
1 0 0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	20000
1 0 1	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	20400
1 1 0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	22000
1 1 1	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	22400
0 0 0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	24000
0 0 1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	24400
0 1 0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	26000
0 1 1	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	26400
1 0 0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	28000
1 0 1	1	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	28400
1 1 0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	30000
1 1 1	1	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	30400
0 0 0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	32000
0 0 1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	32400
0 1 0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	34000
0 1 1	1	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	34400
1 0 0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	36000
1 0 1	1	1	1	1	0	1	1	0	1	0	0	0	0	0	0	0	36400
1 1 0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	38000
1 1 1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	38400
0 0 0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	40000
0 0 1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	40400
0 1 0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	42000
0 1 1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	42400
1 0 0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	44000
1 0 1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	44400
1 1 0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	46000
1 1 1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	46400
0 0 0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	48000
0 0 1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	48400
0 1 0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	50000
0 1 1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	50400
1 0 0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	52000
1 0 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	52400
1 1 0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	54000
1 1 1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	54400

See manual for Octal and Decimal addressing table
 Note: "0" indicates switch is off or open
 "1" indicates switch is on or closed

Address bit	ADDR						OFFS					
	15	14	13	12	11	10	15	14	13	12	11	10
Switch position	6	5	4	3	2	1	6	5	4	3	2	1



* IC73 Optional. Not included in Kit.
 Special Application see manual

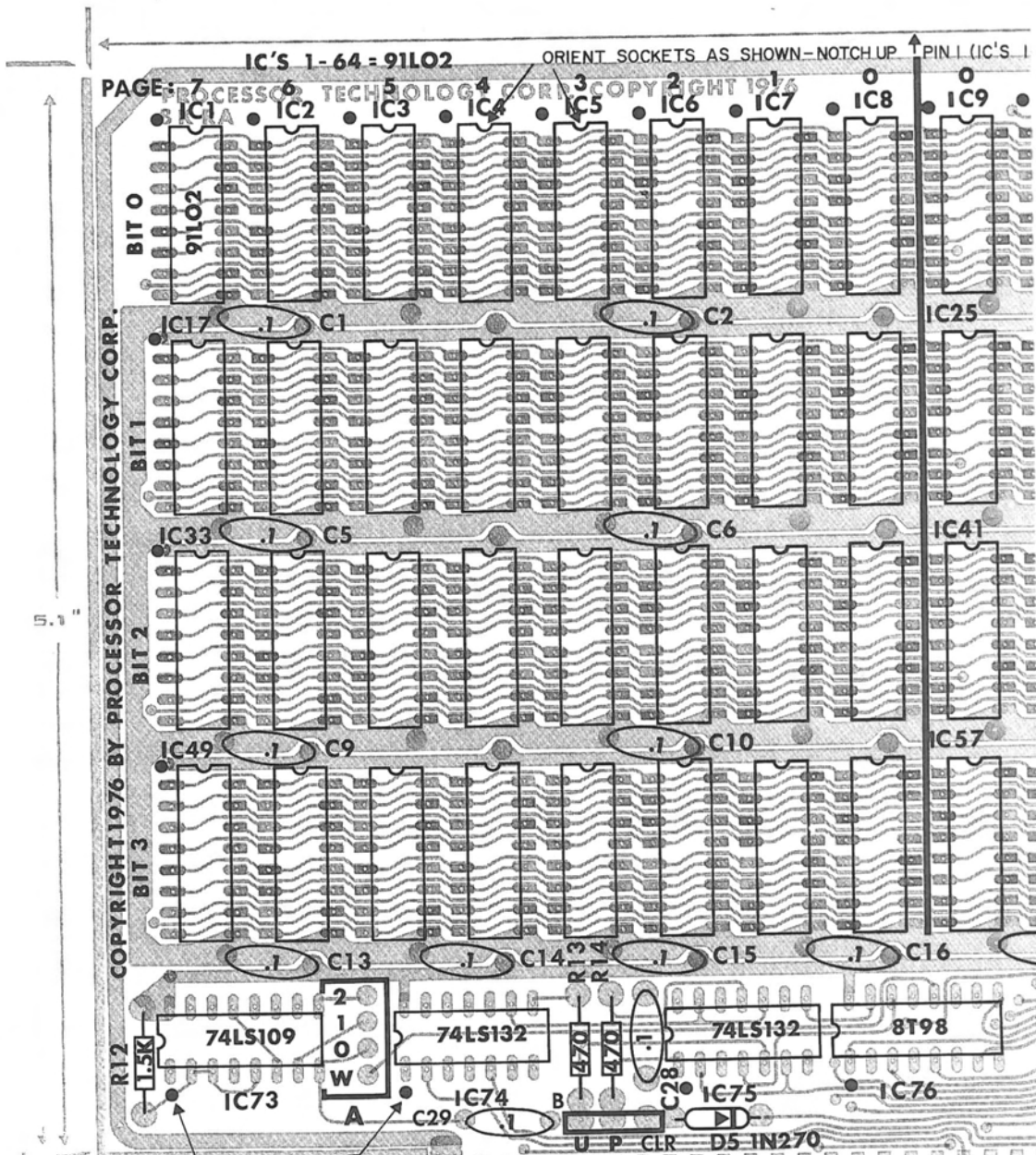


8KRA Schematic

SCALE: 806-C	Designed by: Robert M. Marsh	DRAWN BY: Roeder
DATE: 4/76		REVISED:

Processor Technology Corp.
 8192 x 8 bit low power static RAM board
 Designed to be used with 8080 processors

Board rev (B)
Dwg rev (A)



IC'S 1-64 = 91102
 ORIENT SOCKETS AS SHOWN - NOTCH UP
 PIN 1 (IC'S 1-64)

PAGE: 7

BIT 0

BIT 1

BIT 2

BIT 3

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5.1"

1.5"

6.375"

DOTS MARK PIN 1
 PIN 1 (IC'S 67-79)

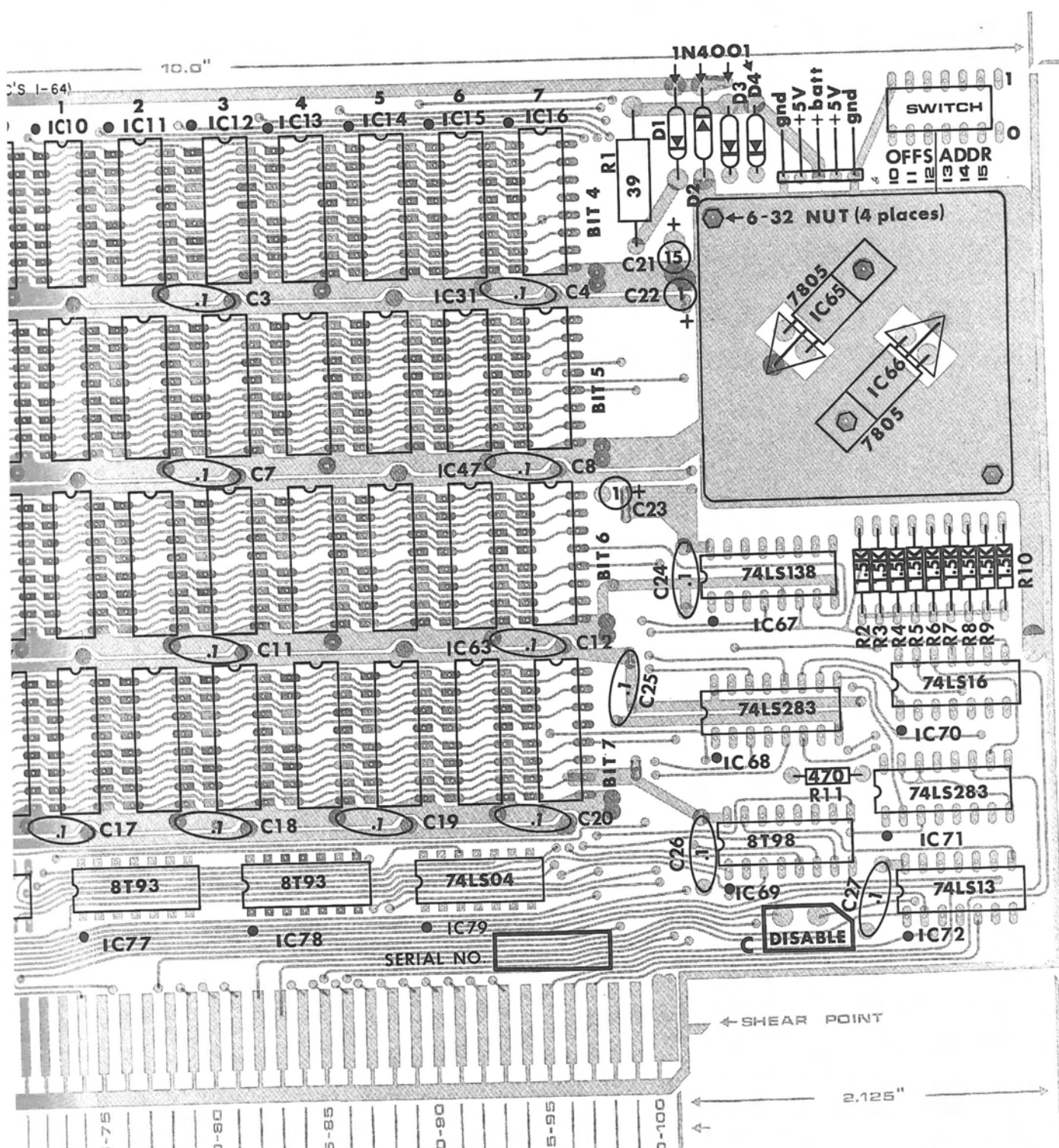
DESIGNED BY: MARSH
 DATE: 1-26-76
 LAYOUT BY: SCHMIDT
 DATE: 3-76
 REVISION: MARSH
 DATE: 7-76

1	3	6
---	---	---

COMPONENT WIRING

+8	+B	1-51
+16	-16	
XRDY	SSW DBS	
V10	EXT CLR	
V11	5-55	
V12		
V13		
V14		
V15		
V16	10-60	
V17		
		15-65
		PHANTOM
		STA DBS - MWRT
		C/C DBS - PS
		UNPROC - PROC
		SS RUN
		ADD DBS - PRDY

U P CLR D5-IN270



SS	RUN
ADD	DSB -PROY
DO	DSB -PINT
μ2	CLK -PHOLD
μ1	CLK -PRESET -25-75
PHLDA	PSYNC
PWAIT	PWR
PINTE	POBIN
A5	A0
A4	A1
A3	A2
A15	A6
A12	A7
A9	A8
DD 1	A13 -35-85
DD 0	A14
A10	A11
DD 4	DD 2
DD 5	DD 3
DD 6	DD 7
DI 2	DI 4
DI 3	DI 5
DI 7	DI 6
SMI	DI 1
SOUT	DI 0
SINP	SINTA
SMER	SWO
SHLTA	SSTACK
CLOCK	POC
GND	GND -50-100

Processor Technology Corporation
 6200 Hollis Street (415) 652-8080
 Emeryville, Ca 94608

STANDARD CARD OUTLINE
 Copyright 1976

Title: **8K RA FOIL ASSEMBLY** Rev: **C**
 Side: **BOTH FRONT**

APPENDICES

- I Warranty Information
- II 8080 Operating Code
- III Soldering Tips
- IV Standard Color Code for Resistors
and Capacitors
- V Integrated Circuit Pin Configurations
- VI Memory Test Programs



Warranty

PROCESSOR TECHNOLOGY CORPORATION, in recognition of its responsibility to provide quality components and adequate instruction for their proper assembly, warrants its products as follows:

All components sold by **Processor Technology Corporation** are purchased through normal factory distribution and any part which fails because of defects in workmanship or material will be replaced at no charge for a period of 3 months for kits, and one year for assembled modules, following the date of purchase. The defective part must be returned postpaid to **Processor Technology Corporation** within the warranty period.

Any malfunctioning module, purchased as a kit and returned to **Processor Technology** within the warranty 3 month period, which in the judgement of **PTCO** has been assembled with care and not subjected to electrical or mechanical abuse, will be restored to proper operating condition and returned, regardless of cause of malfunction, with a minimal charge to cover postage and handling.

Any modules purchased as a kit and returned to **PTCO** which in the judgement of **PTCO** are not covered by the above conditions will be repaired and returned at a cost commensurate with the work required. In no case will this charge exceed \$20.00 without prior notification and approval of the owner.

Any modules, purchased as assembled units are guaranteed to meet specifications in effect at the time of manufacture for a period of at least one year following purchase. These modules are additionally guaranteed against defects in materials or workmanship for the same one year period. All warranted factory assembled units returned to **PTCO** postpaid will be repaired and returned without charge.

This warranty is made in lieu of all other warranties expressed or implied and is limited in any case to the repair or replacement of the module involved.



Processor Technology Corporation
6200 Hollis Street
Emeryville CA 94608

SOLDERING TIPS

- (1) Use a low-wattage iron -- 25 watts is good. Larger irons run the risk of burning the printed-circuit board. Don't try to use a soldering gun, they are too hot.
- (2) Use a small pointed tip and keep it clean. Keep a damp piece of sponge by the iron and wipe the tip on it after each use.
- (3) Use 60-40 rosin-core solder ONLY. DO NOT use acid-core solder or externally applied fluxes. Use the smallest diameter solder you can get.

NOTE: DO NOT PRESS THE TOP OF THE IRON ON THE PAD OR TRACE. THIS WILL CAUSE THE TRACE TO "LIFT" OFF OF THE BOARD WHICH WILL RESULT IN PERMANENT DAMAGE.

- (4) In soldering, wipe the tip, apply a light coating of new solder to it, and apply the tip to both parts of the joint, that is, both the component lead and the printed-circuit pad. Apply the solder against the lead and pad being heated, but not directly to the tip of the iron. Thus, when the solder melts the rest of the joint will be hot enough for the solder to "take," (i.e., form a capillary film).
- (5) Apply solder for a second or two, then remove the solder and keep the iron tip on the joint. The rosin will bubble out. Allow about three or four bubbles, but don't keep the tip applied for more than ten seconds.
- (6) Solder should follow the contours of the original joint. A blob or lump may well be a solder bridge, where enough solder has been built upon one conductor to overflow and "take" on the adjacent conductor. Due to capillary action, these solder bridges look very neat, but they are a constant source of trouble when boards of a high trace density are being soldered. Inspect each integrated circuit and component after soldering for bridges.
- (7) To remove solder bridges, it is best to use a vacuum "solder puller" if one is available. If not, the bridge can be reheated with the iron and the excess solder "pulled" with the tip along the printed circuit traces until the lump of solder becomes thin enough to break the bridge. Braid-type solder remover, which causes the solder to "wick-up" away from the joint when applied to melted solder, may also be used.

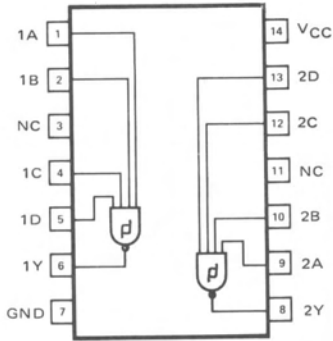
STANDARD COLOR CODE FOR RESISTORS AND CAPACITORS

COLOR	SIGNIFICANT FIGURE	DECIMAL MULTIPLIER	TOLERANCE (%)	VOLTAGE RATING*
Black	0	1		--
Brown	1	10		100
Red	2	100		200
Orange	3	1,000		300
Yellow	4	10,000		400
Green	5	100,000		500
Blue	6	1,000,000		600
Violet	7	10,000,000		700
Gray	8	100,000,000		800
White	9	1,000,000,000		900
Gold	-	0.1	5	1000
Silver	-	0.01	10	2000
No Color	-	---	20	500

*Applies to capacitors only.

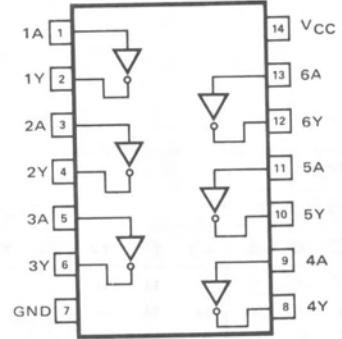
INTEGRATED CIRCUIT PIN CONFIGURATIONS

74LS13



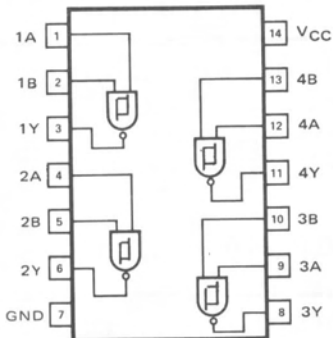
POSITIVE LOGIC: $Y = \overline{ABCD}$

74LS04 or 8T93



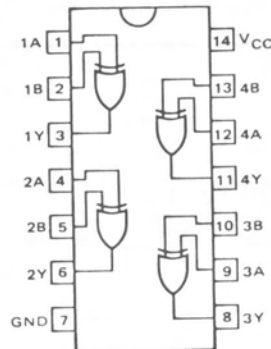
POSITIVE LOGIC: $Y = \overline{A}$

74LS132



POSITIVE LOGIC: $Y = \overline{AB}$

74LS136



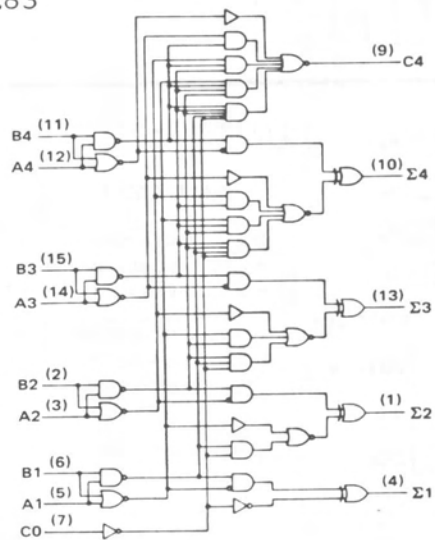
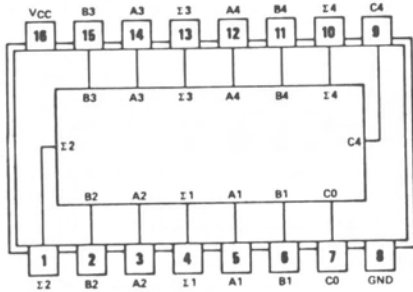
positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

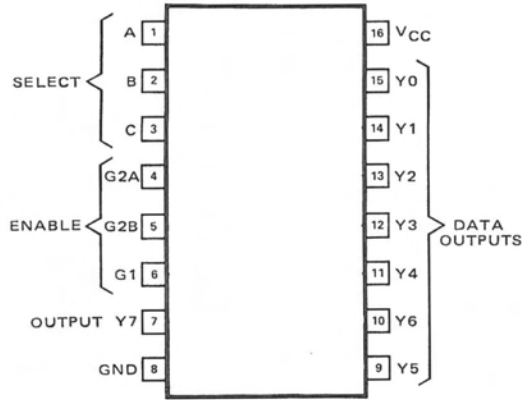
H = high level; L = low level

SN74LS283



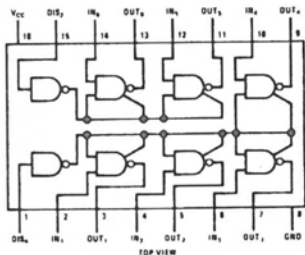
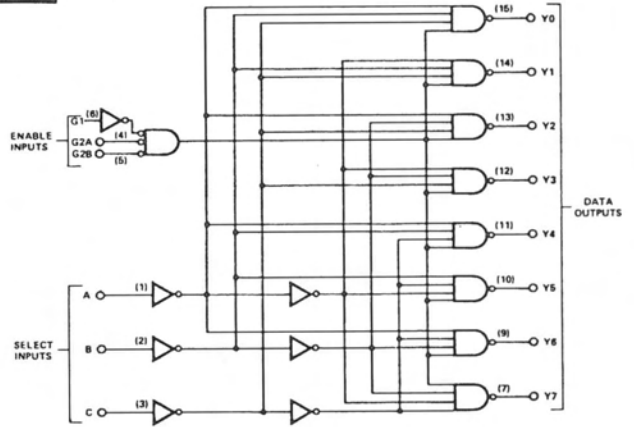
74LS138

positive logic: see function table



INPUTS			OUTPUTS								
ENABLE	SELECT			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
G1	G2*	C	B	A							
X	H	X	X	X	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	H	H	H	H	H	H	H	H	L

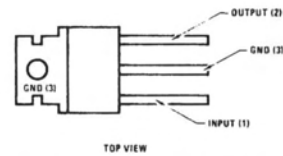
*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant



8098 or 8T98

DISABLE DIS ₄	INPUT DIS ₂	INPUT	OUTPUT
0	0	0	1
0	0	1	0
X	1	X	H _z *
1	X	X	H _z **

*Output 5-6 only
**Output 1-4 only
X = Irrelevant

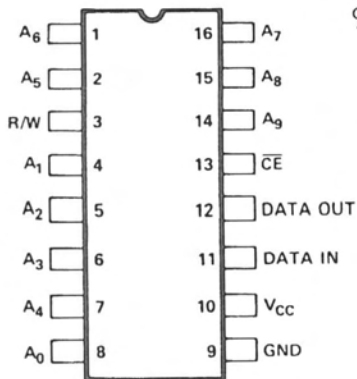


LM340T-5.0 or 7805UC

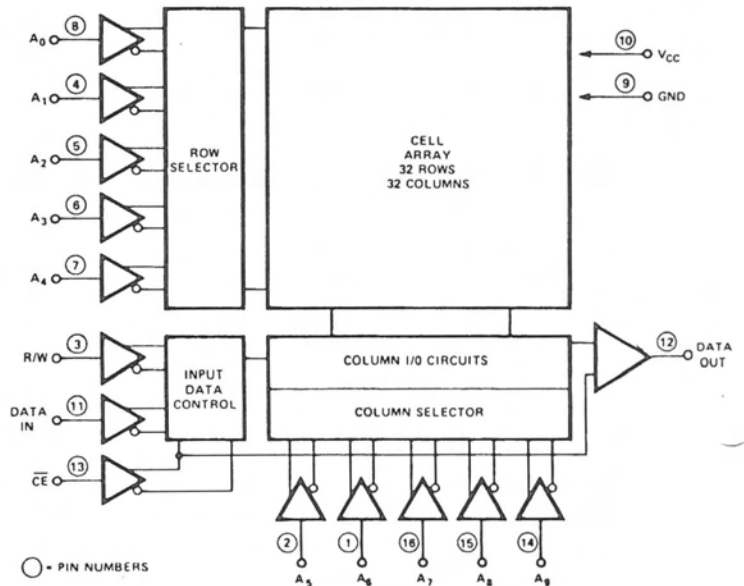
91LO2A or 21LO2B

PIN NAMES

D _{IN}	DATA INPUT
A ₀ A ₉	ADDRESS INPUTS
R/W	READ/WRITE INPUT
CE	CHIP ENABLE
D _{OUT}	DATA OUTPUT
V _{CC}	POWER (+5V)



91LO2A or 21LO2B
BLOCK DIAGRAM



VI.1 SHORT 8K MEMORY TEST

The short 8K memory test will find most errors in any 8K segment of memory. The long 8K MEMORY TEST very thoroughly tests any 8K segment of memory and also prints out a map which identifies the probable bad memory IC. The short test is useful since it does not require a terminal.

The short test is performed in two segments: write and read. Write begins at the bottom of the 8K address (LOAD), writing zero and then writing an incrementing pattern to the "top". After each location is read and compared to its proper pattern, and if no errors are found, the starting pattern is incremented and the test is once again performed.

This read-write sequence continues until an error is found or until the machine is halted. If an error is found, all information relating to the error is saved in locations 000 - 006.

ADDRESS

1	High Address Error Pointer
2	Low Address Error Pointer
3	Write Data
4	Read Data (Error)
5	Page Down Count

VI.1.1 Test Procedure

To use the test program given in Paragraph V.1.2, proceed as follows:

- () Step 1. Clear memory locations 0000 through 0006 and load the hex code starting from location 0007.
- () Step 2. As the code is entered, check the address for each input as a test of proper code and location.
- () Step 3. Check each location for the proper bits after a all code is entered.
- () Step 4. Press RESET and RUN switches. The test should proceed as indicated by the address lights.

NOTE

A full test of all 256 bit patterns to all 8192 locations takes about one minute with a fast memory.

- () Step 5. Repeat test for one hour with the computer cover in place

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APPENDIX VI

VI.1.2 8K SHORT MEMORY TEST PROGRAM

me/m
not/c

func

```

0000
0000
0000
0000
0000
0000
0000
0000
0000
0000
0007 31 06 00
000A AF
000B 47
000C
000C 21 00 20
000F 48
0010 71
0011 23
0012 0C
0013 7C
0014 FE 40
0016 C2 10 00
0019
0019
0019
0019 78
001A 0E 04
001C 21 00 20
001F
001F 11 00 04
0022 BE
0023 C2 3B 00
0026 1D
0027 C2 2E 00
002A 15
002B CA 33 00
002E
002E 23
002F 3C
0030 C3 22 00
0033
0033 0D
0034 C2 1F 00
0037 04
0038 C3 0C 00
003B
003B
003B
003B
003B
003B

```

```

0000 * <<< 8K MEMORY TEST PROGRAM >>>
0001 *
0002 * ASSEMBLED ON SOFTWARE PACKAGE #1
0008 LOAD EQU 8192
0009 TOP EQU 64
0010 SP EQU 6
0015 *
0020 ORG 7
0025 *
0030 START LXI SP, 6 SET UP ERROR CATCH
0035 XRA A CLEAR REG A
0040 MOV B,A CLEAR B
0045 *
0050 OVER LXI H, LOAD LOAD ADDRESS
0053 MOV C,B FIRST WRITE DATA
0055 WRITE MOV M,C PUT IN MEMORY
0060 INX H NEXT ADDR
0065 INR C NEXT WRITE DATA
0070 MOV A,H
0075 CPI TOP IS H OVER THE TOP?
0080 JNZ WRITE IF NOT THEN MORE
0081 *
0082 * READ TEST ROUTINE
0083 *
0085 MOV A,B GET FIRST WRITE DATA
0090 MVI C,4 C HOLDS PAGE COUNT
0095 LXI H, LOAD LOAD ADDRESS
0096 *
0100 NEXT LXI D, 1024 D-E COUNT K'S
0110 READ CMP M IS DATA OK?
0112 JNZ ERROR IF NOT CATCH IT
0115 DCR E
0118 JNZ OKTES
0120 DCR D ANOTHER PAGE DOWN
0125 JZ ONEK COUNT K'S
0133 *
0135 OKTES INX H NEXT ADDRESS
0140 INR A
0145 JMP READ
0146 *
0150 ONEK DCR C ONE MORE K DOWN
0155 JNZ NEXT MORE K'S TO COUNT
0157 INR B
0160 JMP OVER
0170 *
0175 * ERROR STUFF ROUTINE
0180 *
0185 * ADDRESS
0186 * 5 HAS HIGH ERROR ADDR
0187 * 4 HAS LOW " "

```

003B		0188	*	3	HAS WRITE DATA
003B		0189	*	2	HAS READ DATA (ERROR)
003B		0190	*	0	HAS PAGE DOWN COUNT
003B		0210	*		
003B		0215	*		
003B	E5	0216	ERROR		PUSH H STUFF ADDRESSES
003C	57	0220			MOV D,A GET WRITE DATA
003D	5E	0225			MOV E,M GET READ DATA
003E	D5	0230			PUSH D PUT ON STACK
003F	C5	0235			PUSH B ALL OF IT
0040	76	0240	AHHHH		HLT STOP THIS NONSENSE
0041		0245	*		
0041		0250	*		

VI.2 8KRA LONG MEMORY TEST

This test requires a terminal which has an ESCAPE function. It provides a more thorough test than the short test and also prints out a map which simplifies identification of defective components.

VI.2.1 Test Procedure

To use the 8KRA Long Memory Test, proceed as follows:

NOTE 1

The 8KRA to be tested MUST be unprotected. Also, the address offset switches (A10, A11 and A12) on the 8KRA to be tested MUST all be in the off position. They remain in this position throughout the entire test.

NOTE 2

The test program will defeat attempts to test the lowest 8K of memory which contains the test program itself.

- () Step 1. Set DIP Switches A15, A14 and A13 on the 8KRA as described in Section III, Paragraph 3.5 of this manual to select one of these starting addresses: 2000, 4000, 6000, 8000, A000, C000 or E000 (all hex).

NOTE 1

The 8KRA to be tested MUST be addressed at one of the seven preceding addresses.

() Step 1. (continued)

NOTE 2

When the 8KRA is not being tested, it can be addressed at any of the sixty-four 1K intervals specified in Table 3-1 in Section III of this manual.

- () Step 2. Load test program into memory starting at location 0000.
- () Step 3. Set the starting address selected in Step 1 for the 8KRA to be tested into Sense Switches 13 through 15. (These Sense Switches are set to the highest order bits that are recognized by the 8KRA under test; namely A15, A14 and A13.) Sense Switch settings for the seven possible starting addresses are as follows:

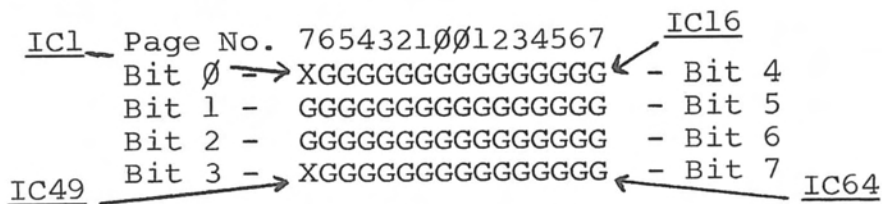
ADDRESS (Hex)	SENSE SWITCH SETTINGS		
	15	14	13
2000	Down	Down	Up
4000	Down	Up	Down
6000	Down	Up	Up
8000	Up	Down	Down
A000	Up	Down	Up
C000	Up	Up	Down
E000	Up	Up	Up

- () Step 4. Start test by pressing RESET and RUN Switches in that order.

NOTE

The test takes several minutes to run. When the test is done, a print routine will print a map that corresponds to the memory IC layout of the 8KRA board; that is, four rows of sixteen.

- () Step 5. Analyze the map to determine which bits are defective. An example follows:



A "G" indicates all bits in the corresponding IC memory (IC16, for example) are good. An "X" indicates that one or more of the bits in the corresponding IC memory (IC49, for example) are defective. A defective bit, or bits, can be caused by a bad IC memory or a defect in one or more of the decoding and interface IC's.

() Step 6. The test may be repeated by striking the ESCAPE key.

NOTE

To test another 8KRA, set new address into Sense Switches and strike ESCAPE key.

VI.2.2 LONG 8K MEMORY TEST PROGRAM

```

0000                                1000 ***** 8KRA TEST PROGRAM *****
0000                                1005 *
0000                                1010 * 2/24/1976
0000                                1015 * WRITTEN BY LORIN S. MOHLER
0000                                1020 *
0000                                1025 * MAPPING ROUTINES WRITTEN BY
0000                                1030 * VERN MUHR
0000                                1035 *
0000                                1040 * ASSEMBLED ON THE: ALS-8 SOFTWARE
0000                                1045 * DEVELOPMENT SYSTEM
0000                                1050 *
0000 F3                                1055          DI          DISABLE INTERRUPTS
0001 DB 01                            1060          IN          KBDI          CLEAR KEYBOARD READY
0003 31 D2 01                        1065 BGIN LXI          SP,AREA+20H /RESTARTING POINT
0006 CD 3E 00                        1070          CALL         CRLF          RESTART FROM ESC
0009 DB FF                            1075 INSS          IN          OFFH          READ SENSE SWITCHES
000B E6 E0                            1080          ANI          OEOH          MASK LOWER FIVE
000D CA 09 00                        1085          JZ          INSS          NOT ALLOWED
0010 67                                1090          MOV          H,A          SET UP START ADDRESS
0011 2E 00                            1095          MVI          L,0
0013 22 82 01                        1100          SHLD         BBUF          STORE START ADDRESS
0016 21 00 00                        1105          LXI          H,0          CLEAR MAP AREA
0019 22 78 01                        1110          SHLD         EBUF
001C 22 7A 01                        1115          SHLD         EBUF+2
001F 22 7C 01                        1116          SHLD         EBUF+4
0022 22 7E 01                        1117          SHLD         EBUF+6
0025                                1120 *
0025 2A 82 01                        1125          LHLD         BBUF
0028 3E 20                            1130          MVI          A,20H
002A 84                                1135          ADD          H          END=START+8K
002B 67                                1140          MOV          H,A
002C 2B                                1145          DCX          H
002D 22 84 01                        1150          SHLD         BBUF+2 /STORE END ADRS
0030 C3 68 00                        1155          JMP          MRCK          BEGIN TEST
0033                                1160 *
0033 DB 00                            1165 OUT8          IN          VIDS          READ I/O STATUS
0035 E6 80                            1170          ANI          80H
0037 CA 33 00                        1175          JZ          OUT8          WAIT

```


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APPENDIX VI

003A	78		1180		MOV	A,B		
003B	D3	01	1185		OUT	VIDO	XMIT DATA	
003D	C9		1190		RET			
003E			1195	*				
003E	06	0D	1200	CRLF	MVI	B,13	WRITE CR LF & 2 RUBOUTS	
0040	CD	33 00	1205		CALL	OUT8		
0043	06	0A	1210		MVI	B,10		
0045	CD	33 00	1215		CALL	OUT8		
0048	06	7F	1220		MVI	B,127		
004A	CD	33 00	1225		CALL	OUT8		
004D	CD	33 00	1230		CALL	OUT8		
0050	C9		1235		RET			
0051			1240	*				
0051	2A	82 01	1245	ACHK	LHLD	BBUF	FETCH ADDRESS	
0054	3A	85 01	1250		LDA	BBUF+3	STOP ADDRESS	
0057	BC		1255		CMP	H	COMPARE HIGH ADDRESS	
0058	C2	63 00	1260		JNZ	ACH1		
005B	3A	84 01	1265		LDA	BBUF+2	STOP ADDRESS LOW	
005E	BD		1270		CMP	L		
005F	C2	63 00	1275		JNZ	ACH1		
0062	37		1280		STC		SET CARRY IF EQUAL	
0063			1285	*				
0063	23		1290	ACH1	INX	H	INCREMENT START ADDRESS	
0064	22	82 01	1295		SHLD	BBUF	STORE INCR START ADDRESS	
0067	C9		1300		RET			
0068			1305	*				
0068	21	01 00	1310	MRCK	LXI	H,1	INITIALIZE PASS COUNT	
006B	22	96 01	1315		SHLD	DBUF+4	STORE IT	
006E	2A	82 01	1320	MRC1	LHLD	BBUF	GET START LOCATION	
0071	E5		1325		PUSH	H	SAVE START LOCATION	
0072	AF		1330		XRA	A	INITIALIZE MASTER PATTERN	
0073	37		1335		STC		SET CARRY	
0074	F5		1340		PUSH	PSW	STORE MASTER PATTERN	
0075			1345	*				
0075	F5		1350	WRL1	PUSH	PSW	SAVE WORKING PATTERN	
0076	77		1355		MOV	M,A	PATTERN 1 TO MEMORY	
0077	CD	51 00	1360		CALL	ACHK	CHECK IF LAST, INCREMENT LOCA	
007A	DA	82 00	1365		JC	RDL1	DONE WRITING PATTERN	
007D	F1		1370		POP	PSW	GET WORKING PATTERN	
007E	17		1375		RAL		SHIFT WORKING PATTERN	
007F	C3	75 00	1380		JMP	WRL1	DO MORE WRITING	
0082			1385	*				
0082	F1		1390	RDL1	POP	PSW	UNLOAD STACK	
0083	F1		1395		POP	PSW	GET MASTER PATTERN	
0084	E1		1400		POP	H	RESTORE START LOCATION	
0085	22	82 01	1405		SHLD	BBUF	STORE START	
0088	E5		1410		PUSH	H	SAVE START	
0089	F5		1415		PUSH	PSW	SAVE MASTER PATTERN	
008A			1420	*				
008A	F5		1425	RDL2	PUSH	PSW	SAVE WORKING PATTERN	
008B	BE		1430		CMP	M	CHECK IT	
008C	C4	FA 00	1435		CNZ	MTER	READ ERROR	
008F	CD	EB 00	1440		CALL	ESCP	CHECK FOR ESCAPE	
0092	CD	51 00	1445		CALL	ACHK	O/ENCE LOCATION. CHECK IF LAS	
0095	DA	9D 00	1450		JC	NXP1	NEXT PATTERN 1	
0098	F1		1455		POP	PSW	GET WORKING PATTERN	

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APPENDIX VI

0099	17		1460		RAL		SHIFT WORKING PATTERN
009A	C3	8A 00	1465		JMP	RDL2	DO MORE
009D			1470	*			
009D	F1		1475	NXP1	POP	PSW	UNLOAD STACK
009E	F1		1480		POP	PSW	GET MASTER PATTERN
009F	17		1485		RAL		SHIFT STARTING PATTERN
00A0	DA	AC 00	1490		JC	TST2	TEST 1 IS COMPLETE. DO TEST 2
00A3	E1		1495		POP	H	GET START
00A4	22	82 01	1500		SHLD	BBUF	STORE START
00A7	E5		1505		PUSH	H	SAVE START
00A8	F5		1510		PUSH	PSW	SAVE MASTER PATTERN
00A9	C3	75 00	1515		JMP	WRL1	CONTINUE TEST 1
00AC			1520	*			
00AC	E1		1525	TST2	POP	H	RESTORE START ADDR
00AD	22	82 01	1530		SHLD	BBUF	STORE START ADDRESS
00B0	E5		1535		PUSH	H	SAVE START ADDRESS
00B1	AF		1540		XRA	A	INITIALIZE MASTER PATTERN
00B2	37		1545		STC		SET CARRY
00B3	F5		1550		PUSH	PSW	SAVE MASTER PATTERN
00B4			1555	*			
00B4	F5		1560	WRL2	PUSH	PSW	SAVE WORKING PATTERN
00B5	77		1565		MOV	M,A	WRITE PATTERN TO MEMORY
00B6	CD	51 00	1570		CALL	ACHK	INCR LOCATION, AND CHECK IF LA
00B9	DA	C1 00	1575		JC	RDL3	DONE WRITING
00BC	F1		1580		POP	PSW	RESTORE PATTERN
00BD	1F		1585		RAR		SHIFT PATTERN
00BE	C3	B4 00	1590		JMP	WRL2	DO MORE
00C1			1595	*			
00C1	F1		1600	RDL3	POP	PSW	UNLOAD STACK
00C2	F1		1605		POP	PSW	GET MASTER PATTERN
00C3	E1		1610		POP	H	GET START
00C4	22	82 01	1615		SHLD	BBUF	STORE START
00C7	E5		1620		PUSH	H	SAVE START
00C8	F5		1625		PUSH	PSW	SAVE MASTER PATTERN
00C9			1630	*			
00C9	F5		1635	RDL4	PUSH	PSW	SAVE PATTERN
00CA	BE		1640		CMP	M	CHECK IT
00CB	C4	FA 00	1645		CNZ	MTER	ERROR
00CE	CD	EB 00	1650		CALL	ESCP	CHECK FOR ESCAPE
00D1	CD	51 00	1655		CALL	ACHK	INCR LOCATION CHECK IF LAST
00D4	DA	DC 00	1660		JC	NXP2	NEXT PATTERN
00D7	F1		1665		POP	PSW	GET WORKING PATTERN
00D8	1F		1670		RAR		SHIFT WORKING PATTERN
00D9	C3	C9 00	1675		JMP	RDL4	DO MORE READING
00DC			1680	*			
00DC	F1		1685	NXP2	POP	PSW	UNLOAD STACK
00DD	F1		1690		POP	PSW	GET MASTER PATTERN
00DE	1F		1695		RAR		SHIFT PATTERN
00DF	DA	10 01	1700		JC	MTCP	MEMORY TEST COMPLETE MESSAGE
00E2	E1		1705		POP	H	RESTORE START
00E3	22	82 01	1710		SHLD	BBUF	STORE START
00E6	E5		1715		PUSH	H	SAVE START
00E7	F5		1720		PUSH	PSW	SAVE MASTER PATTERN
00E8	C3	B4 00	1725		JMP	WRL2	DO MORE
00EB			1730	*			
00EB	DB	00	1735	ESCP	IN	VIDS	ANYBODY KNOCK?
00ED	E6	40	1740		ANI	40H	STATUS MASK
00EF	C8		1745		RZ		NO, CONTINUE

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APPENDIX VI

00F0	DB	01	1750	IN	KBDI	YES, WHAT WAS IT?
00F2	E6	7F	1755	ANI	7FH	PARITY MASK
00F4	FE	1B	1760	CPI	1BH	ESC 7
00F6	CA	03 00	1765	JZ	BGIN	RESTART
00F9	C9		1770	RET		NOT AN ESCAPE, CONTINUE
00FA			1775	*		
00FA			1780	*	THIS ROUTINE MAPS	ERRORS
00FA			1785	*	INTO EBUF AREA	
00FA			1790	*		
00FA	D1		1795	MTER	POP	D
00FB	F1		1800		POP	PSW /GET WRITE PATTERN
00FC	F5		1805		PUSH	PSW
00FD	D5		1810		PUSH	D
00FE	AE		1815		XRA	M /EXOR READ PATTERN
00FF	47		1820		MOV	B,A /SAVE IN B
0100	3A	83 01	1825		LDA	BBUF+1
0103	E6	1C	1830		ANI	1CH
0105	0F		1835		RRC	
0106	0F		1840		RRC	
0107	21	78 01	1845		LXI	H,EBUF
010A	85		1850		ADD	L /COMPUTE MAP POINTER
010B	6F		1855		MOV	L,A
010C	7E		1860		MOV	A,M
010D	B0		1865		ORA	B /PUT ERRORS IN MAP
010E	77		1870		MOV	M,A
010F	C9		1875		RET	
0110			1880	*		
0110			1885	*	GET HERE WHEN PASS COMPLETE	
0110			1890	*		
0110	3A	96 01	1895	MTCP	LDA	DBUF+4
0113	3C		1900		INR	A
0114	32	96 01	1905		STA	DBUF+4
0117	FE	04	1910		CPI	4
0119	CA	23 01	1915		JZ	MAP8 AFTER 4 PASSES
011C	E1		1920		POP	H
011D	22	82 01	1925		SHLD	BBUF
0120	C3	6E 00	1930		JMP	MRC1
0123			4000	*		
0123			4001	*	THIS ROUTINE PRINTS THE MAP	
0123			4002	*		
0123	21	7F 01	4005	MAP8	LXI	H,ERUF+7
0126	16	40	4010		MVI	D,64
0128	1E	11	4015		MVI	E,11H LOAD THE REG'S.
012A	0E	0F	4020		MVI	C,0FH
012C	CD	4C 01	4025	BACK	CALL	MOUT PRINT 8 CHAR'S.
012F	CD	4C 01	4035		CALL	MOUT PRINT 8 MORE
0132	AF		4040		XRA	A
0133	BA		4045		CMP	D DONE YET ?
0134	C2	43 01	4046		JNZ	NOPE
0137	CD	3E 00	4048		CALL	CRLF DONE !!!
013A	CD	3E 00	4050		CALL	CRLF
013D	CD	EB 00	4052	LOOP3	CALL	FSCP
0140	C3	3D 01	4054		JMP	LOOP3
0143	7B		4058	NOPE	MOV	A,E
0144	07		4060		RLC	READY FOR NEXT ROW
0145	5F		4065		MOV	F,A
0146	CD	3E 00	4067		CALL	CRLF
0149	C3	2C 01	4070		JMP	BACK FOR MORE

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8KRA STATIC READ/WRITE MEMORY MODULE

APPENDIX VI

014C	7E	6000	MOUT	MOV	A,M		
014D	A3	6005		ANA	E	AND BIT MASK	
014E	A1	6010		ANA	C	AND COLUMN MASK	
014F	06 47	6015		MVI	R,'G'		
0151	CA 56 01	6020		JZ	PAST		
0154	06 58	6025		MVI	R,'X'		
0156	CD 33 00	6026	PAST	CALL	OUT8	PRINT 'X' OR 'G'	
0159	15	6027		DCR	D		
015A	3E 07	6028		MVI	A,07H		
015C	A2	6029		ANA	D		
015D	CA 6D 01	6030		JZ	FLIP	PREPARE FOR NEXT 8 COLS	
0160	79	6031		MOV	A,C		
0161	17	6032		RAL	TEST COLUMN MASK		
0162	DA 69 01	6033		JC	UP		
0165	2B	6034		DCX	H		
0166	C3 4C 01	6035		JMP	MOUT UNTIL 8 CHARS.		
0169	23	6036	UP	INX	H		
016A	C3 4C 01	6040		JMP	MOUT UNTIL 8 CHARS		
016D	79	6045	FLIP	MOV	A,C		
016E	EE FF	6050		XRI	OFFH		
0170	4F	6055		MOV	C,A		
0171	C9	6060		RET			
0172		6065	*				
0172	00	6070	FIN	NOP		BUFFERS START HERE	
0173		6075	*				
0173		6080	EBUF	EQU	FIN+6H		
0173		6085	RBUF	EQU	FIN+10H	BINARY BUFFER	
0173		6090	DBUF	EQU	FIN+20H		
0173		6095	AREA	EQU	FIN+40H	STACK AREA	
0173		6096	VIDS	EQU	0	STATUS PORT	
0173		6097	VIDO	EQU	1	DATA PORT	
0173		6098	KBDI	EQU	VIDO		
0173		6099	SP	EQU	6		
0173		7000	PSW	EQU	6		

ACH1	0063	ACHK	0051	AREA	01B2	BACK	012C
BBUF	0182	BGIN	0003	CRLF	003E	DRUF	0192
EBUF	0178	ESCP	00EB	FIN	0172	FLIP	016D
INSS	0009	KBDI	0001	LOOP3	013D	MAP8	0123
MOUT	014C	MRC1	006E	MRCK	0068	MTCP	0110
MTER	00FA	NOPE	0143	NXP1	009D	NXP2	00DC
OUT8	0033	PAST	0156	PSW	0006	RDL1	0082
RDL2	008A	RDL3	00C1	RDL4	00C9	SP	0006
TST2	00AC	UP	0169	VIDO	0001	VIDS	0000
WRL1	0075	WRL2	00B4				

HEX-ASCII TABLE		Printing	Characters
00	NOP	30	0
01	LXI B,D16	31	1
02	STAX B	32	2
03	INX B	33	3
04	INR B	34	4
05	DCR B	35	5
06	MVI B,D8	36	6
07	RLC	37	7
08	...	38	8
09	DAD B	39	9
0A	LDAX B	41	A
0B	DCX B	42	B
0C	INR C	43	C
0D	DCR C	44	D
0E	MVI C,D8	45	E
0F	RRC	46	F
10	...	47	G
11	LXI D,D16	48	H
12	STAX D	49	I
13	INX D	4A	J
14	INR D	4B	K
15	DCR D	4C	L
16	MVI D,D8	4D	M
17	RAL	4E	N
18	...	4F	O
19	DAD D	50	P
1A	LDAX D	51	Q
1B	DCX D	52	R
1C	INR E	53	S
1D	DCR E	54	T
1E	MVI E,D8	55	U
1F	RAR	56	V
20	...	57	W
21	LXI H,D16	58	X
22	SHLD Adr	59	Y
23	INX H	5A	Z
24	INR H		
25	DCR H		
26	MVI H,D8		
27	DAA		
28	...		
29	DAD H		
2A	LHLD Adr		
2B	DCX H		
2C	INR L		
2D	DCR L		
2E	MVI L,D8		
2F	CMA		
30	...		
31	LXI SP,D16		
32	STA Adr		
33	INX SP		
34	INR M		
35	DCR M		
36	MVI M,D8		
37	STC		
38	...		
39	DAD SP		
3A	LDA Adr		
3B	DCX SP		
3C	INR A		
3D	DCR A		
3E	MVI A,D8		
3F	CMC		
40	MOV B,B		
41	MOV B,C		
42	MOV B,D		
43	MOV B,E		
44	MOV B,H		
45	MOV B,L		
46	MOV B,M		
47	MOV B,A		
48	MOV C,B		
49	MOV C,C		
4A	MOV C,D		
4B	MOV C,E		
4C	MOV C,H		
4D	MOV C,L		
4E	MOV C,M		
4F	MOV C,A		
50	MOV D,B		
51	MOV D,C		
52	MOV D,D		
53	MOV D,E		
54	MOV D,H		
55	MOV D,L		
56	MOV D,M		
57	MOV D,A		
58	MOV E,B		
59	MOV E,C		
5A	MOV E,D		
5B	MOV E,E		
5C	MOV E,H		
5D	MOV E,L		
5E	MOV E,M		
5F	MOV E,A		
60	MOV H,B		
61	MOV H,C		
62	MOV H,D		
63	MOV H,E		
64	MOV H,H		
65	MOV H,L		
66	MOV H,M		
67	MOV H,A		
68	MOV L,B		
69	MOV L,C		
6A	MOV L,D		
6B	MOV L,E		
6C	MOV L,H		
6D	MOV L,L		
6E	MOV L,M		
6F	MOV L,A		
70	MOV M,B		
71	MOV M,C		
72	MOV M,D		
73	MOV M,E		
74	MOV M,H		
75	MOV M,L		
76	HLT		
77	MOV M,A		
78	MOV A,B		
79	MOV A,C		
7A	MOV A,D		
7B	MOV A,E		
7C	MOV A,H		
7D	MOV A,L		
7E	MOV A,M		
7F	MOV A,A		
80	ADD B		
81	ADD C		
82	ADD D		
83	ADD E		
84	ADD H		
85	ADD L		
86	ADD M		
87	ADD A		
88	ADC B		
89	ADC C		
8A	ADC D		
8B	ADC E		
8C	ADC H		
8D	ADC L		
8E	ADC M		
8F	ADC A		
90	SUB B		
91	SUB C		
92	SUB D		
93	SUB E		
94	SUB H		
95	SUB L		
96	SUB M		
97	SUB A		
98	SBB B		
99	SBB C		
9A	SBB D		
9B	SBB E		
9C	SBB H		
9D	SBB L		
9E	SBB M		
9F	SBB A		
A0	ANA B		
A1	ANA C		
A2	ANA D		
A3	ANA E		
A4	ANA H		
A5	ANA L		
A6	ANA M		
A7	ANA A		
A8	XRA B		
A9	XRA C		
AA	XRA D		
AB	XRA E		
AC	XRA H		
AD	XRA L		
AE	XRA M		
AF	XRA A		
B0	ORA B		
B1	ORA C		
B2	ORA D		
B3	ORA E		
B4	ORA H		
B5	ORA L		
B6	ORA M		
B7	ORA A		
B8	CMP B		
B9	CMP C		
BA	CMP D		
BB	CMP E		
BC	CMP H		
BD	CMP L		
BE	CMP M		
BF	CMP A		
C0	RNZ		
C1	POP B		
C2	JNZ Adr		
C3	JMP Adr		
C4	CNZ Adr		
C5	PUSH B		
C6	ADI D8		
C7	RST 0		
C8	RZ		
C9	RET		
CA	JZ		
CB	...		
CC	CZ		
CD	CALL		
CE	ACI D8		
CF	RST 1		
D0	RNC		
D1	POP D		
D2	JNC		
D3	OUT D8		
D4	CNC		
D5	PUSH D		
D6	SUI D8		
D7	RST 2		
D8	RC		
D9	...		
DA	JC		
DB	IN D8		
DC	CC		
DD	...		
DE	SBI D8		
DF	RST 3		
E0	RPO		
E1	POP H		
E2	JPO Adr		
E3	XTHL		
E4	CPO Adr		
E5	PUSH H		
E6	ANI D8		
E7	RST 4		
E8	RPE		
E9	PCHL		
EA	JPE Adr		
EB	XCHG		
EC	CPE Adr		
ED	...		
EE	XRI D8		
EF	RST 5		
F0	RP		
F1	POP PSW		
F2	JP Adr		
F3	DI		
F4	CP Adr		
F5	PUSH PSW		
F6	ORI D8		
F7	RST 6		
F8	RM		
F9	SPHL		
FA	JM Adr		
FB	EI		
FC	CM Adr		
FD	...		
FE	CPI D8		
FF	RST 7		

HEX-ASCII TABLE

HEX-ASCII TABLE		Non-Printing
00	NULL	
07	BELL	
09	TAB	
0A	LF	
0B	VT	
0C	FORM	
0D	CR	
11	X-ON	
12	TAPE	
13	X-OFF	
14	ESC	
1B	ESC	
7D	ALT MODE	
7F	RUB OUT	

D8 = constant, or logical/arithmetic expression that evaluates to an 8 bit data quantity.
 D16 = constant, or logical/arithmetic expression that evaluates to a 16 bit data quantity.
 Adr = 16 bit address



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