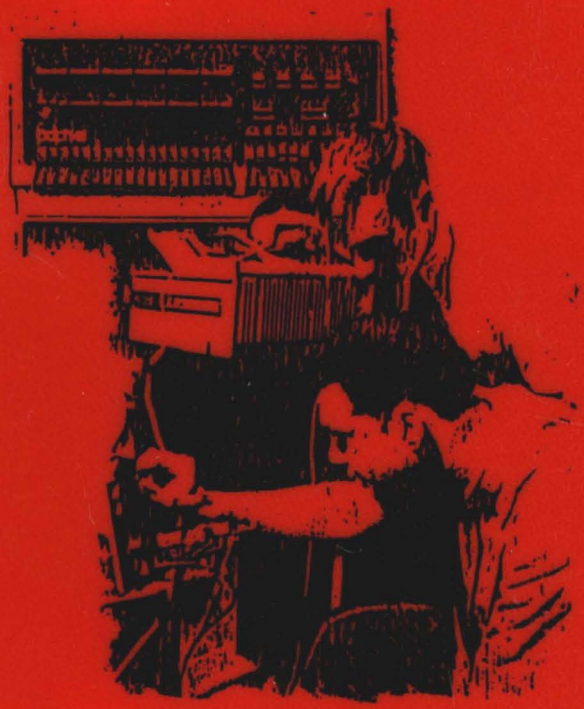
pdp11
Mainframe

Troubleshooting Guide



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PDP-11 Mainframe Troubleshooting Guide

(Flows and DECAIDS)

COMPANY CONFIDENTIAL

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CONTENTS (Cont)

THE PDP-11 MAINFRAME TROUBLESHOOTING GUIDE

INTRODUCTION

This guide is comprised of two major sections:

1. The Troubleshooting Flowchart
2. The DECAIDs.

It is intended that they be used concurrently by Field Service personnel to aid them in locating and repairing faults in PDP-11 systems that utilize PDP-11/05/10/35/40/45 CPUs.

The guide makes two basic assumptions.

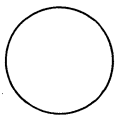
1. The Field Service technician has an excellent supply of replacement parts (e.g., modules, power regulators, cables, etc.).

2. There is a configured copy of DEC/X11 with the system which has been loaded and run error-free at some time prior to this failure. That is, the system has already been installed and was fully operational at one time. The guide does not provide the necessary information on how to install either systems or add-ons to a system.

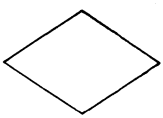
THE TROUBLESHOOTING FLOWCHART

The flows guide the Field Service technician through the steps he must perform to isolate a fault to either a peripheral device or the mainframe and if it is found to be in the mainframe, then to either the Unibus, power system, internal option, memory, or processor. Once the fault has been isolated, the flows then indicate the steps to follow to repair the fault on a field-replaceable-unit basis.

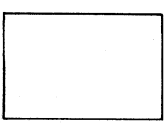
The symbology used in the flowchart is as follows:



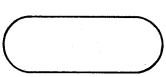
Circle
An entry from or exit to other pages of the flows with the pages listed in parentheses near the circle.



Diamond
A decision point.



Rectangle
A procedure or operation to be performed by the technician.



Bubble
A reference to one of the DECAIDs that provides the technician with the information necessary to perform the operation or make the decision.

The 13 pages of flows are organized as follows:

1.–2. Starting and quick-check; loading and running system exercisers

3.–4. AC power

5.–6. DC power

7. Mainframes

8. Unibus

9.–10. Consoles

11. Processors

12. Memories

13. Peripherals.

The flowchart is intended to fulfill two primary functions.

1. To aid the technician in determining a logical troubleshooting approach to a system failure.

2. To help the technician develop an effective troubleshooting technique.

THE DECAIDS

The second section of the quide provides the troubleshooter with all the information necessary to perform the operations, do the adjustments, and make the decisions to isolate and repair a problem in a PDP-11 system. These DECAIDs cover all the detailed aspects of troubleshooting from how to load a diagnostic to the procedure for adjusting core memory strobes to locating the output pins on a power regulator's connector.

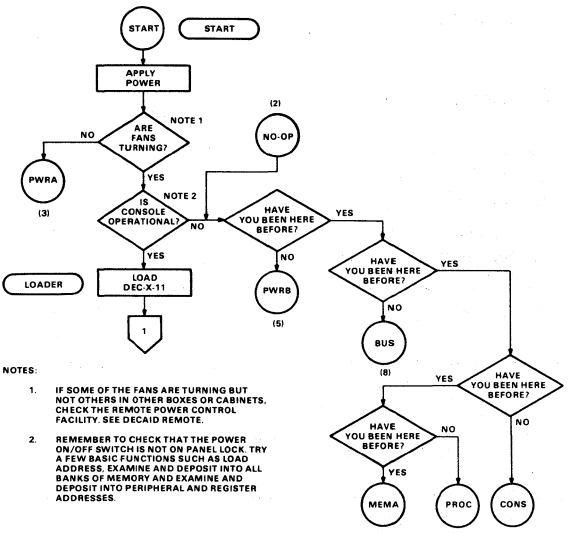
It is intended that these DECAIDs will be used by the technician on the job, providing information that is:

1. Much too detailed to memorize

2. Hidden away in one of more than a dozen manuals and engineering drawings

3. Not available anywhere else.

TROUBLESHOOTING FLOWCHART 1

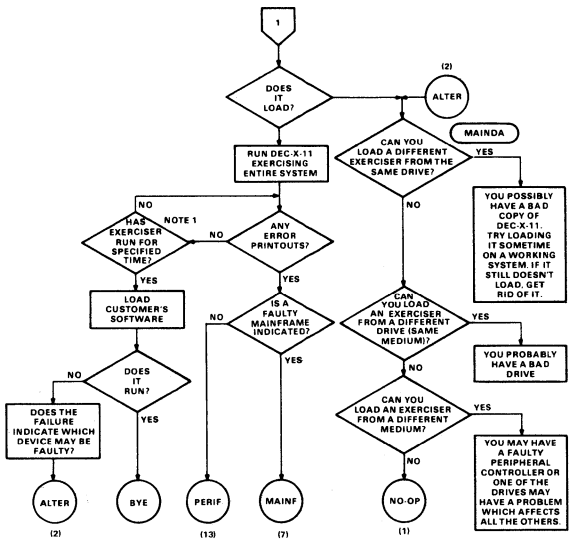


NOTES:

1. IF SOME OF THE FANS ARE TURNING BUT NOT OTHERS IN OTHER BOXES OR CABINETS, CHECK THE REMOTE POWER CONTROL FACILITY. SEE DECAID REMOTE.

2. REMEMBER TO CHECK THAT THE POWER ON/OFF SWITCH IS NOT ON PANEL LOCK. TRY A FEW BASIC FUNCTIONS SUCH AS LOAD ADDRESS, EXAMINE AND DEPOSIT INTO ALL BANKS OF MEMORY AND EXAMINE AND DEPOSIT INTO PERIPHERAL AND REGISTER ADDRESSES.

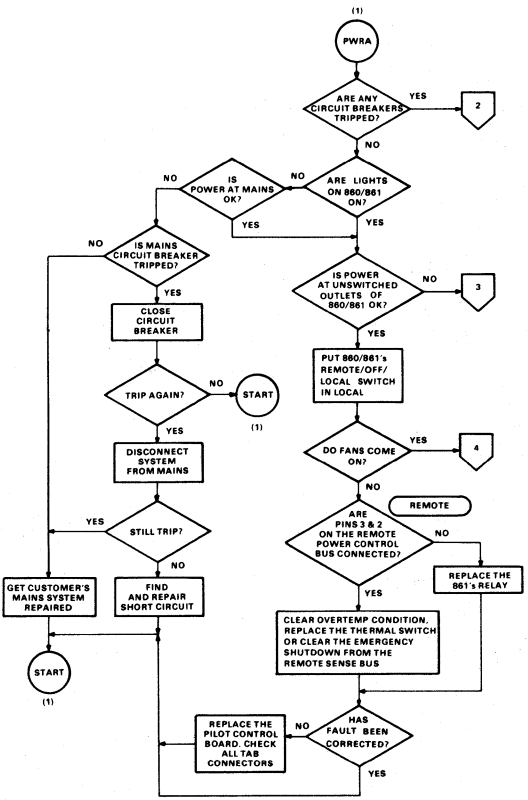
TROUBLESHOOTING FLOWCHART 2



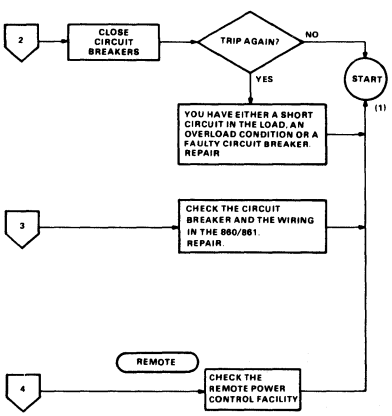
NOTE

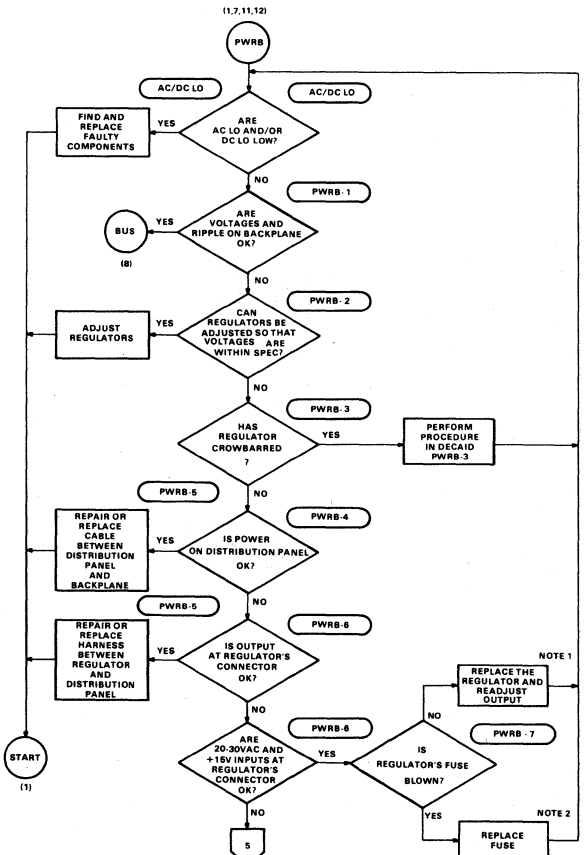
1 WHEN RUNNING A MAINDEC IT IS SOMETIMES DIFFICULT TO DETECT WHETHER IT IS RUNNING PROPERLY OR WHETHER IT IS HUNG IN A LOOP. READ THE MAINDEC'S WRITE-UP TO SEE IF YOU CAN USE SUCH TECHNIQUES AS SETTING UP THE SWITCH REGISTER TO CAUSE A FREQUENT PRINTOUT, EXERCISING THE CONSOLE TERMINAL'S PRINTER, RUNNING IN SINGLE ITERATION MODE, ETC.

TROUBLESHOOTING FLOWCHART 3



TROUBLESHOOTING FLOWCHART 4



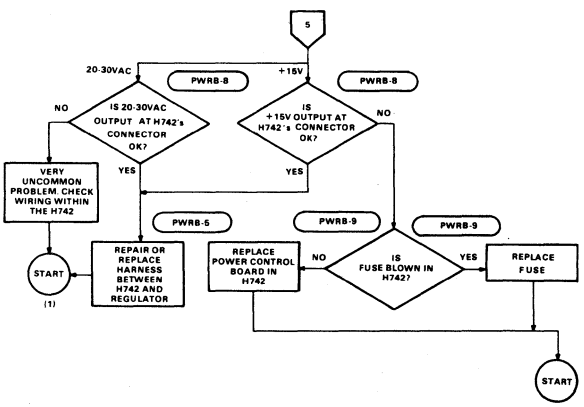


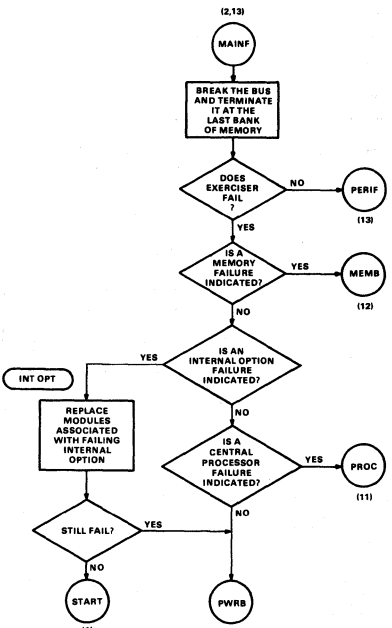
NOTES:

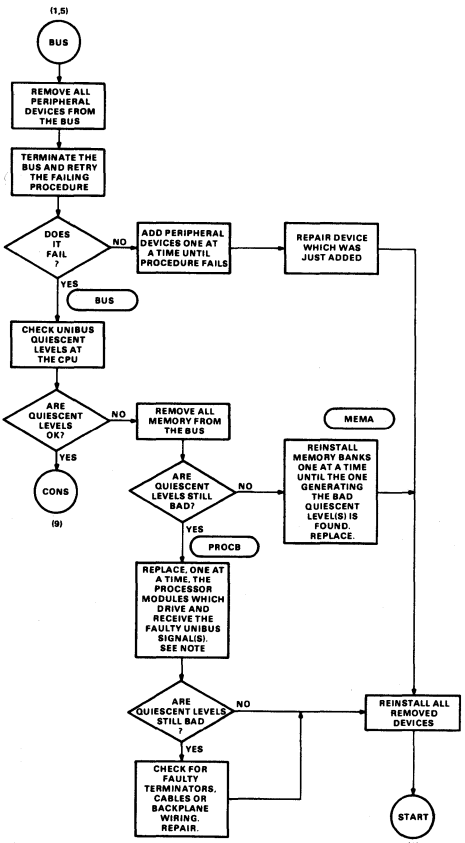
1. Before replacing the fuse or regulator, check for possible causes. Faulty components within the regulator itself can cause the fuse to blow. Check for scorching of the etch board and/or components. Check the backplane for a bent pin or a piece of wire which might be causing a short circuit.

2. If system is an 11/05/10, check the voltages as listed in DECAID PWRD.

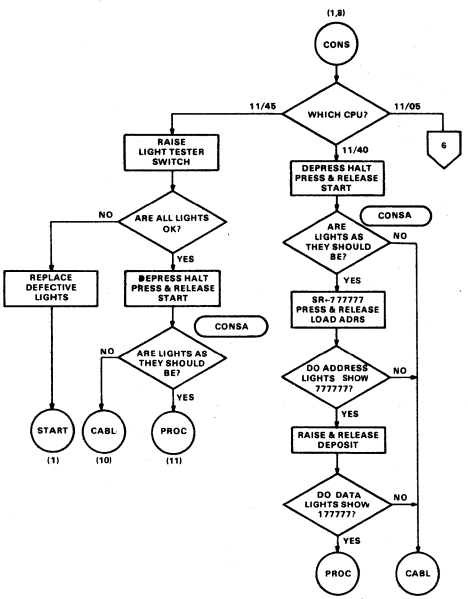
TROUBLESHOOTING FLOWCHART 6

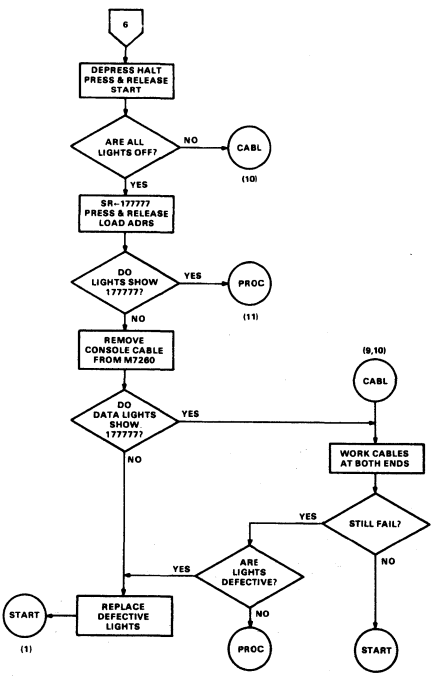


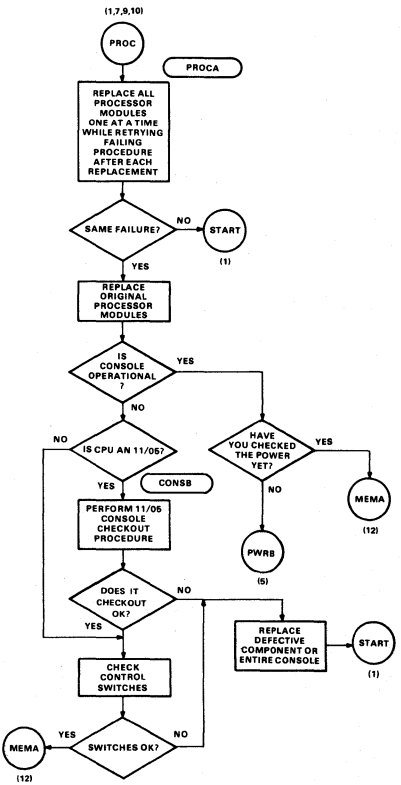

(2,13)
MAINF
BREAK THE BUS AND TERMINATE IT AT THE LAST BANK OF MEMORY
DOES EXERCISER FAIL ?
NO
PERIF
(13)
YES
IS A MEMORY FAILURE INDICATED?
YES
MEMB
(12)
NO
IS AN INTERNAL OPTION FAILURE INDICATED?
YES
INT OPT
REPLACE MODULES ASSOCIATED WITH FAILING INTERNAL OPTION
NO
IS A CENTRAL PROCESSOR FAILURE INDICATED?
YES
PROC
(11)
NO
STILL FAIL?
YES
NO
START
(1)
PWRB
(5)

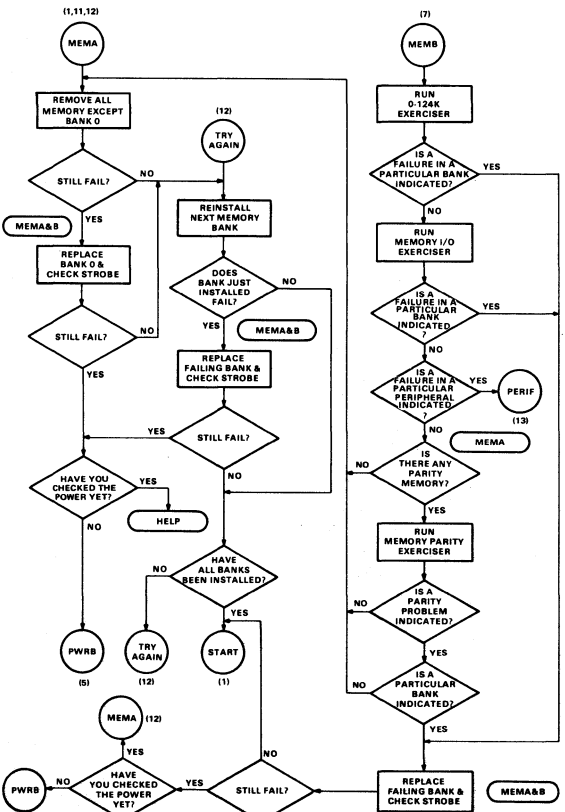


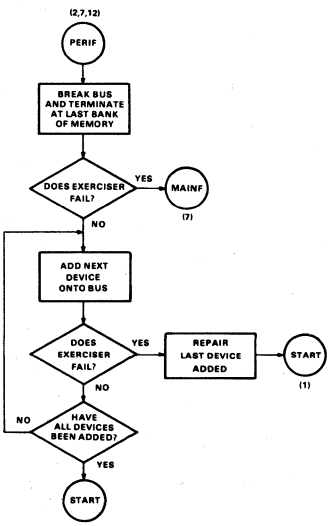
NOTE:
REMEMBER, AC LO AND DC LO ARE ALSO POWER SUPPLY DEPENDENT.


(1,8)
CONS
WHICH CPU?
11/45
11/05
11/40
6
RAISE LIGHT TESTER SWITCH
DEPRESS HALT PRESS & RELEASE START
NO
ARE ALL LIGHTS OK?
YES
REPLACE DEFECTIVE LIGHTS
DEPRESS HALT PRESS & RELEASE START
CONSA
NO
ARE LIGHTS AS THEY SHOULD BE?
YES
START
(1)
CABL
(10)
PROC
(11)
CONSA
ARE LIGHTS AS THEY SHOULD BE?
NO
YES
SR=777777 PRESS & RELEASE LOAD ADRS
DO ADDRESS LIGHTS SHOW 7777777
NO
YES
RAISE & RELEASE DEPOSIT
DO DATA LIGHTS SHOW 177777?
NO
YES
PROC
(11)
CABL
(10)


6
DEPRESS HALT
PRESS & RELEASE
START
ARE ALL
LIGHTS OFF?
NO
CABL
(10)
YES
SR=177777
PRESS & RELEASE
LOAD ADRS
DO
LIGHTS SHOW
177777?
YES
PROC
(11)
NO
REMOVE
CONSOLE CABLE
FROM M7260
DO
DATA LIGHTS
SHOW
177777?
YES
NO
(9,10)
CABL
WORK CABLES
AT BOTH ENDS
STILL FAIL?
YES
NO
ARE
LIGHTS
DEFECTIVE?
YES
NO
START
(1)
REPLACE
DEFECTIVE
LIGHTS
PROC
(11)
START
(1)


(1,7,9,10)
PROC
PROCA
REPLACE ALL PROCESSOR MODULES ONE AT A TIME WHILE RETRYING FAILING PROCEDURE AFTER EACH REPLACEMENT
SAME FAILURE?
NO
START
(1)
YES
REPLACE ORIGINAL PROCESSOR MODULES
IS CONSOLE OPERATIONAL ?
YES
NO
IS CPU AN 11/05?
NO
YES
CONSB
PERFORM 11/05 CONSOLE CHECKOUT PROCEDURE
HAVE YOU CHECKED THE POWER YET?
YES
NO
MEMA
(12)
PWRB
(5)
DOES IT CHECKOUT OK?
NO
YES
REPLACE DEFECTIVE COMPONENT OR ENTIRE CONSOLE
START
(1)
CHECK CONTROL SWITCHES
YES
NO
SWITCHES OK?
MEMA
(12)


(1,11,12)
MEMA
REMOVE ALL MEMORY EXCEPT BANK 0
STILL FAIL?
NO
YES
MEMA&B
REPLACE BANK 0 & CHECK STROBE
STILL FAIL?
NO
YES
HAVE YOU CHECKED THE POWER YET?
YES
HELP
NO
PWRB
(5)
(12)
TRY AGAIN
REINSTALL NEXT MEMORY BANK
DOES BANK JUST INSTALLED FAIL?
NO
YES
MEMA&B
REPLACE FAILING BANK & CHECK STROBE
STILL FAIL?
YES
NO
HAVE ALL BANKS BEEN INSTALLED?
NO
YES
TRY AGAIN
(12)
START
(1)
MEMA (12)
YES
HAVE YOU CHECKED THE POWER YET?
NO
YES
PWRB
(5)
STILL FAIL?
NO
YES
(7)
MEMB
RUN 0-124K EXERCISER
IS A FAILURE IN A PARTICULAR BANK INDICATED?
YES
NO
RUN MEMORY I/O EXERCISER
IS A FAILURE IN A PARTICULAR BANK INDICATED?
YES
NO
IS A FAILURE IN A PARTICULAR PERIPHERAL INDICATED?
YES
PERIF
(13)
NO
MEMA
IS THERE ANY PARITY MEMORY?
NO
YES
RUN MEMORY PARITY EXERCISER
IS A PARITY PROBLEM INDICATED?
NO
YES
IS A PARTICULAR BANK INDICATED?
NO
YES
REPLACE FAILING BANK & CHECK STROBE
MEMA&B


(2,7,12)
PERIF
BREAK BUS AND TERMINATE AT LAST BANK OF MEMORY
DOES EXERCISER FAIL?
YES
MAINF
(7)
NO
ADD NEXT DEVICE ONTO BUS
DOES EXERCISER FAIL?
YES
REPAIR LAST DEVICE ADDED
START
(1)
NO
HAVE ALL DEVICES BEEN ADDED?
NO
YES
START
(1)

LOCATION OF AC LO/DC LO SIGNALS

Signal	11/05	11/40*	11/45*
	M7261	M7235	M8106
AC LO	B08F1	B06D2	C12S1
DC LO	B08F2 (Very difficult to scope. Check on tab connector)	B06C1	C12U1

Quiescent levels should be +4.8 V ± 0.2 V

AC LO and DC LO are generated in the above CP modules, the bulk power supplies, and the power supplies of all peripherals. These are all connected to the Unibus in a wired OR. The processor receives them and makes itself and its memories totally inoperative if either one is true. It, therefore, will be necessary to physically disconnect the system in a logical fashion to determine which device is faulty.

* The following displays will be seen on the front panel if DC LO is true:

PDP-11/45 – The CPU's microaddress will be 200.

PDP-11/40 – The CONS and RUN lights will be off and the BUS and PROC lights will be on.

QUIESCENT UNIBUS LEVELS

Normal bus quiescent levels are listed below. Any level that deviates from normal should be looked upon as a potential failure. In most cases, this improper level will be caused by a defective bus receiver or driver. AC LO and DC LO are also power-supply dependent.

Signal	Quiescent Level
BG(7:4), NPG, BBSY (on PDP-11/40)	+0.4 V ± 0.4 V
AC LO, DC LO	+4.8 V ± 0.2 V
All others	+3.4 V ± 0.2 V

Procedure

To measure quiescent Unibus levels:

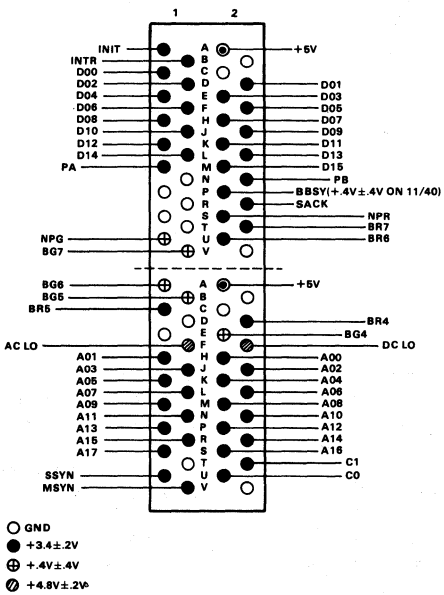
1. Turn the system on with the processor halted. Press the START key and release it with HALT down. (On older PDP-11/40s it is necessary to LOAD ADRS 000000 to clear the A<17:00> lines.)

2. Use a *calibrated* oscilloscope to measure the Unibus signal lines. (See the following chart of Unibus slot backplane pins.)

To obtain meaningful readings of bus grant lines (BG<7:4> and NPG), they should be measured at *each* device wired to them down the length of the bus.

All buses should be checked in multiple bus systems.

UNIBUS SLOT
(Viewed from the Backplane)



QUIESCENT CONSOLE LIGHT DISPLAY

Press and release the START key with the HALT key down.

PDP-11/40

ADRS = 000000
DATA = 000000
RUN = ON
BUS = ON
PROC = ON
CONSOLE = ON
All the rest = OFF

PDP-11/45

All ADRS = 000000
DISPLAY REG = 000000
BUS REG = 000000
DATA PATHS = Contents of R0
μADRS CPU = 170 (200 when START is held down)
KERNEL = ON (OFF when START is held down)
MASTER = ON
All the rest = OFF

PDP-11/05 CONSOLE CHECKOUT PROCEDURE

1. Make certain the computer power is off.

2. Disconnect the console cable connector from the M7260 module and then turn on the computer power.

3. After step 2 is completed, the data pattern 177777_8 should be displayed on the console lights.

4. At the connector that plugs into the M7260 module, use a piece of small gauge wire and jumper pin F to the following pins and observe if the displayed pattern is correct. Remove the jumper each time before proceeding to the next step.

5. Jumper: GND; Pattern: 000000

6. Jumper: N; Pattern: 125252

7. Jumper: L; Pattern: 146314

8. Jumper: J; Pattern: 170360

9. Jumper: D; Pattern: 177400

10. Remove the jumper after completing the procedure.

WHAT TO DO WHEN ALL ELSE FAILS

Most of the cases in the flowchart that take you here are for problem symptoms that are very unusual. Make sure you have checked every possibility. If you have a solid problem and you just don't know where to go, start at NO-OP on flow page 1.

PROCESSOR'S INTERNAL OPTIONS

PDP-11/05

None

PDP-11/40

KE11-E	Extended Instruction Set M7238, slot 2 Requires jumper changes; see DECAID PROCA40
KE11-F	Floating Instruction Set M7239, slot 1 Requires jumper changes; see DECAID PROCA40
KT11-D	Memory Management M7236, slot 8 Requires jumper changes; see DECAID PROCA40
KJ11-A	Stack Limit Register M7237, slot 3E Requires jumper changes; see DECAID PROCA40
KW11-L	Line Clock M787, slot 3F Requires wire change; see DECAID PROCA40

PDP-11/45

FP11	Floating Point Processor M8114, slot 2 M8115, slot 3 M8112, slot 4 M8113, slot 5 No jumper changes required.
KT11-C	Memory Management M8108, slot 13 M8107, slot 14 Requires removal of M8116 from slot 14
KW11-L	Line Clock M787, slot 1C Requires removal of wire between pin C01R2 and pin C01V2.

FOR SYSTEMS EQUIPPED WITH PAPER TAPE

NOTE

In the following descriptions, the value XX reflects the system's memory size as shown below:

Memory Size	XX
4K	01
8K	03
12K	05
16K	07
20K	11
24K	13
28K or greater	15

LOAD ADRS.....XX7744
DEPOSIT.....016701
000026
012702
000352
005211
105711
100376
116162
000002
XX7400
005267
177756
000765
177560 (TTY)
or 177550 (PC11)

Place the Absolute Loader tape in the specified reader with the special bootstrap leader code (ASCII code 351) over the reader sensors.

LOAD ADRS XX7744
START

The Absolute Loader tape will pass through the reader and will stop when the last frame of data has been loaded into memory.

Place the MAINDEC tape in the specified reader with blank leader tape over the reader sensors.

Press CONT or
LOAD ADRS XX7500
START

The MAINDEC tape will pass through the reader and will stop when completely loaded into memory.

At this time R0 which is displayed in the DATA display* will contain all zeros in the low byte. If not, a checksum error has occurred indicating that some data was incorrectly loaded. The tape should be reloaded.

FOR SYSTEMS EQUIPPED WITH DISK, DECtape, AND/OR MAGTAPE

Hardware Bootstrap Loaders

The following table describes the procedures for loading the MAINDEC monitors. Ensure that your XXDP medium is on drive 0.

* For PDP-11/05: to read R0, load address 177700 and press EXAM switch.

ROM	Device	Proceduure
BM792-YB	RK11/RK05	LOAD ADRS.....773100 SWITCH REG.....777406 START
	TC11/TU56	LOAD ADRS.....773100 SWITCH REG.....777344 START
MR11-DB	RK11/RK05	LOAD ADRS.....773110 START
	TC11/TU56	LOAD ADRS.....773120 START
	TM11/TU10	LOAD ADRS.....773136 START
	RP11/RP03	LOAD ADRS.....773154 START
BM873-YA	RK11/RK05	LOAD ADRS.....773010 START
	TC11/TU56	LOAD ADRS.....773030 START
	TM11/TU10	LOAD ADRS.....773050 START
	TA11/TU60	LOAD ADRS.....773230 START
	RP11/RP03	LOAD ADRS.....773100 START

ROM	Device	Procedure
BM873-YB	RK11/RK05 (unit zero)	LOAD ADRS.....773030 START
	RK11/RK05 (Unit specified in Switch register)	LOAD ADRS.....773032 START
	TC11/TU56	LOAD ADRS.....773070 START
	TM11/TU10	LOAD ADRS.....773110 START
	TJU16/TU16	LOAD ADRS.....773150 START
	TA11/TU60	LOAD ADRS.....773524 START
	RP11/RP03	LOAD ADRS.....773350 START
	RJP04/RP04	LOAD ADRS.....773350 START
	RJS03/RS03	LOAD ADRS.....773000 START

Software Bootstrap Loaders

If the hardware bootstrap doesn't work, try one of the following software bootstraps depending on your particular syystem configuration.

Device	Procedure
RK11/RK05	LOAD ADRS.....010000
	DEPOSIT.....012737
	000005
	177404
	000001
	LOAD ADRS.....010000
	START
	Wait 1 second.
	LOAD ADRS.....000000
	START
TC11/TU56	LOAD ADRS.....777342
	DEPOSIT.....004003
	DECtape will rewind.
	EXAMINE
	DEPOSIT.....000001
	LOAD ADRS.....000216
	DEPOSIT.....012737
	000005
	177342
	000777
	LOAD ADRS.....000216
	START

Device	Procedure
TM11/TU10	LOAD ADRS.....010000
	DEPOSIT.....005137
	172524
	012737
	060011
	172522
	000777
	012737
	060003
	172522
	000777
	LOAD ADRS.....010000
	START
	Wait 1 second.
	Press HALT switch.
	LOAD ADRS.....010014
	START
	Wait 1 second.
	Press HALT switch.
	LOAD ADRS.....000000
	START

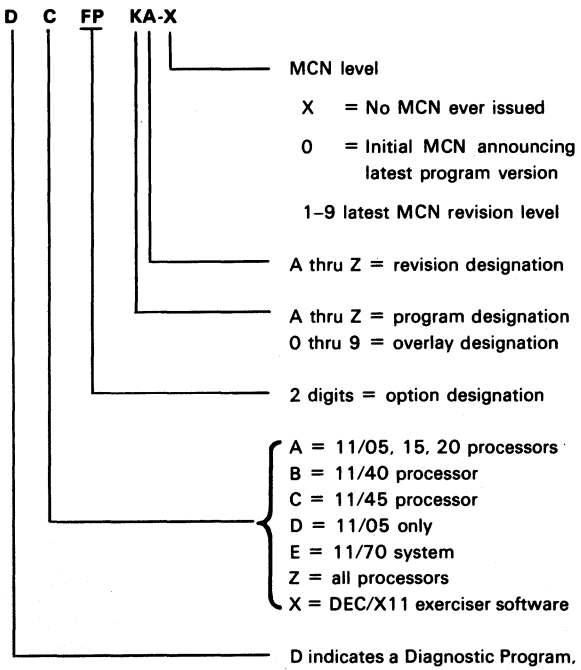
Device	Procedure	
TJU16/TU16	LOAD ADRS	010000
	DEPOSIT	012737
		001300
		172472
		012737
		177777
		172446
		012737
		000031
		172440
		105737
		172452
		100375
		012737
		177400
		172442
		005037
		172444
		042737
		000007
		172452
		012737
		000071
		172440
		105737
		172440
		000100
		000375
		000137
		000000
	LOAD ADRS	010000
	START	

Device	Procedure	
TA11/TU60	LOAD ADRS	001000
	DEPOSIT	012700
		177500
		005010
		010701
		062701
		000052
		012702
		000375
		112103
		112110
		100413
		130310
		001776
		105202
		100772
		116012
		000002
		120337
		000000
		001767
		000000
		000755
		005710
		100774
		005007
		017640
		002415
		112024
	LOAD ADRS	001000
	START	

Device	Procedure
RX11/RX01	LOAD ADRS.....001000
	DEPOSIT.....005000
	012701
	177170
	105711
	001776
	012711
	000003
	005711
	001776
	100405
	105711
	100004
	116120
	000002
	000770
	000000
	005000
	000110
	000000
	000000
	000000
	LOAD ADRS.....001000
	START
RP11/RP03	LOAD ADRS.....001000
	DEPOSIT.....012705
	176716
	012715
	177400
	012745
	000005
	105715
	100376
	005007
	LOAD ADRS.....001000
	START

Device	Procedure	
RJP04/RP04	LOAD ADRS	010000
	DEPOSIT	012700
		176700
		012710
		000023
		005060
		000034
		005060
		000006
		012760
		177400
		000002
		012710
		000071
		105710
		100316
		005007
	LOAD ADRS	010000
	START	
RJS04/RS04	LOAD ADRS	001000
RJS03/RS03	DEPOSIT	012705
		172044
		012745
		177400
		012745
		000071
		032715
		100200
		001775
		100762
		005007
	LOAD ADRS	001000
	START	

MAINDEC NAMING CONVENTION



MAINFRAME MAINDECS AND THE PROCESSORS THEY Run On

Name	Number	05	40	45
CTP Communications	DZQCA	X	X	X
GTP General	DZQGA	X	X	X
T17 4K, CPU, I/O	DZQKB	X	X	X
11 Family Instruction Exerciser	DZQKC	X	X	X
11/40 and 11/45 Instruction Exerciser	DCQKC	–	X	X
Multiplication–Division Exerciser	DCQKA	–	EIS	X
11/40 and 11/45 Processor Parity	DCKBR	–	PAR	PAR
11/45 Console Test	DCKBQ	–	–	X
States 11/45	DCKBO	–	–	X
PIRQ	DCKBN	–	–	X
Traps 11/45	DCKBM	–	–	X
T14 11/05, 20 Traps	DONC	X	–	–
T14 11/40 Traps	DBKDM	–	X	–
Power Fail 11/45	DCKBP	–	–	X
Power Fail 11/05, 20, 40	DZKAQ	X	X	–
DIV	DCKBL	–	EIS	X
MUL	DCKBK	–	EIS	X
ASHC	DCKBJ	–	EIS	X
ASH	DCKBI	–	EIS	X
11/45 Registers	DCKBH	–	–	X
SPL	DCKBG	–	–	X
Stack Limit	DCKBF	–	KJ	X
RTT	DCKBE	–	X	X
MARK	DCKBD	–	X	X
XOR	DCKBC	–	X	X
SOB	DCKBB	–	X	X
SXT	DCKBA	–	X	X

BASIC MAINFRAME MAINDECs (Run On All Processors)

Name	Number
T13 JSR, RTS, RTI	D0MA
T12 Jump	D0LA
T11 Subtract	D0KA
T10 Add	D0JA
T9 Bit Set Clear Test	D0IA
T8 Move	D0HA
T7 CMP Non-Equality	D0GA
T6 CMP Equality	D0FA
T5 Rotate/Shift	D0EA
T4 Binary	D0DA
T3 Unary	D0CA
T2 Con Branch	D0BA
T1 Branch	D0AA

MEMORY MAINDECS AND THE PROCESSORS THEY RUN ON

Name	Number	05	40	45
0–124K Memory Exerciser	DZQMB	X	X	X
Memory I/O Exerciser	DZQMA	X	X	X
Up-Down Address Test	DZMMK	X	X	X
8K Special	DZMMJ	X	X	X
Random Data	DZMMI	X	X	X
Core Heating	DZMMH	X	X	X
Worst Case Noise	DZMMG	X	X	X
Ones Susceptibility	DZMMF	X	X	X
Moving Ones and Zeros	DZMME	X	X	X
Basic Test Patterns	DZMMD	X	X	X
No Dual Address Test	DZMMC	X	X	X
Basic Address Test Down	D1BA	X	X	X
Basic Address Test Up	D1AA	X	X	X
MA11, MF11, and MS11 Parity Test	DCMFA	–	PAR	PAR
MS11	DCMSB	–	–	MOS BIP

INTERNAL OPTION MAINDECS

PDP-11/45 Floating Point – FP11

Name	Number
GTP Overlay	DCQOA
Basic Instruction Exerciser	DCFPO
Division Exerciser	DCFPU
Multiplication Exerciser	DCFPT
Addition and Subtraction Exerciser	DCFPS
LDD/STD Exerciser	DCFPR
Maintenance	DCFPM
MODF, MODD	DCFPL
LDEXP, STEXP	DCFPK
LDCJX, STCXJ	DCFPJ
LDCDF, LDCFD, STCDF, STCFD	DCFPI
CLR, TST, ABS, NEG	DCFPH
DIVF, DIVD	DCFPG
MULF, MULD	DCFPF
CMPF, CMPD	DCFPE
ADDF, ADDD, SUBF, SUBD	DCFPD
LDF, LDD, STF, STD	DCFPC
STS, Illegal Instructions	DCFPB
Basic Test	DCFPA

PDP-11/45 Memory Management – KT11-C

Name	Number
Exerciser	DCKTG
Abort	DCKTF
MFPD/I	DCKTE
MTPD/I	DCKTD
Keys	DCKTC
Logic 2	DCKTB
Logic 1	DCKTA

PDP-11/40 Floating Point – KE11-F

Name	Number
GTP Overlay	DBKEO
Exerciser	DBKEB
Basic Instruction Test	DBKEA

PDP-11/40 Memory Management – KT11-D

Name	Number
Exerciser	DBKTG
Abort	DBKTF
States	DBKTD
MFPI/MTPI	DBKTC
Keys	DBKTB
Logic	DBKTA

Line Clock – KW11-L

Name	Number
Exerciser	DZKWA

PDP-11 SYSTEMS TESTS

1.	DEC/X11	*	2 hours or 2 passes
2.	DZQGA	GTP (for non-communication-oriented systems)* or	2 hours or 2 passes
	DZQCA	CTP (for communication-oriented systems)*	2 hours or 2 passes

* Mechanical devices, e.g., TTY, line printers, should only be run 5 minutes.

PDP-11/05/10 CUSTOMER ACCEPTANCE DIAGNOSTICS

Central Processor

1.	DZQKC	11 Family Instruction Exerciser, any switch 0–7 up	30 minutes
2.	DONC	T14 11/05, 20 traps	2 passes
3.	DZQKB	T17 Systems Test, only console device enabled	10 minutes
4.	DZKAQ	Power Fail	10 power fails

Read/Write Memories

1.	DZQMB	0–124K Memory Exerciser, with switch 11 up	1 minute/8K
2.	DZQMB	0–124K Memory Exerciser, 8K or greater	2 minutes/8K
3.	DZMMI	Random Data, for less than 8K only	5 minutes

PDP-11/35/40 CUSTOMER ACCEPTANCE DIAGNOSTICS

Central Processor

1.	DCQKC	11/40 and 11/45 Instruction Exerciser, any switch 0–7 up	30 minutes
2.	DBKDM	T14 11/40 Traps	2 passes
3.	DZQKB	T17 Systems Test, only console device enabled	10 minutes
4.	DZKAQ	Power Fail	10 power fails

Read/Write Memories

1.	DZQMB	0–124K Memory Exerciser, with switch 11 up	1 minute/8K
2.	DZQMB	0–124K Memory Exerciser, 8K or greater	2 minutes/8K
3.	DCMFA	Parity Test	2 passes

Stack Limit Option – KJ11-A

1.	DCKBF	Stack Limit Option Test	2 minutes

Extended Instruction Set – KE11-E

1.	DCKBI–DCKBL	ASH, ASHC, MUL, DIV Test	2 minutes each
2.	DCQKA	MUL, DIV Random Exerciser	20 minutes

Floating Instruction Set – KE11-F

1.	DBKEB	KE11-F Exerciser	20 minutes
2.	DBKEO	GTP Overlay	20 minutes

Memory Management – KT11-D

1.	DBKTG	KT11-D Exerciser	4 minutes/8K

PDP-11/45/50 CUSTOMER ACCEPTANCE DIAGNOSTICS

Central Processor

1.	DCQKC	11/40 and 11/45 Instruction Exerciser	30 minutes
2.	DZQKB	T17 Systems Test, only console device enabled	10 minutes
3.	DCKBP	Power Fail	1 pass

Read/Write Memories

1.	DZQMB	0–124K Memory Exerciser, with switch 11 up	1 minute/8K
2.	DZQMB	0–124K Memory Exerciser, 8K or greater	2 minutes/8K
3.	DCMFA	Parity Test	2 passes
4.	DCMSB	MOS Memory Test	2 passes

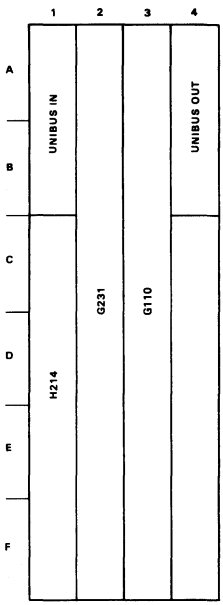
Floating Point Processor – FP11

1.	DZFPO	FP11 Exerciser	20 minutes
2.	DCQOA	GTP Overlay, all available devices enabled except line printer if any	20 minutes

Memory Management – KT11-C

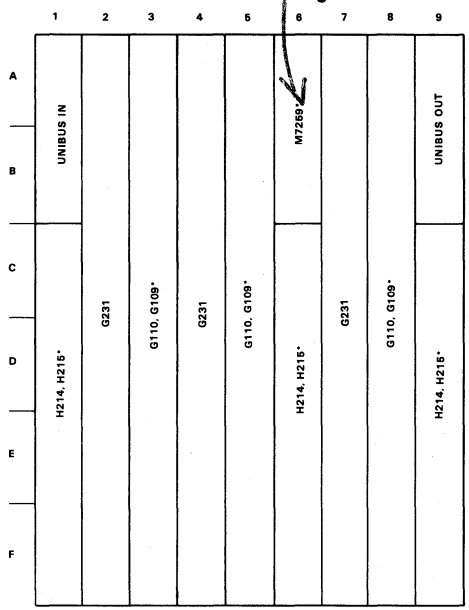
1. DCKTG	KT11-C Exerciser, all available devices enabled except line printer if any	1 pass

MM11-S MODULE UTILIZATION



MF11-L(P) MODULE UTILIZATION

PARITY CONTROLLER



* IF PARITY MEMORY.

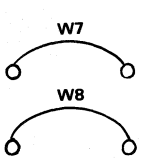
G110 CONTROL MODULE JUMPERS

See the next page for a diagram showing the physical location of the jumpers.

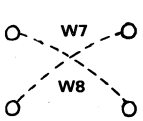
		Device Address Jumpers*			
Memory Bank (words)	Machine Address (words)	W6 A14 or A01†	W4 A15	W3 A16	W2 A17L
0–8K	000000–037776	In	In	In	In
8–16K	040000–077776	Out	In	In	In
16–24K	100000–137776	In	Out	In	In
24–32K	140000–177776	Out	Out	In	In
32–40K	200000–237776	In	In	Out	In
40–48K	240000–277776	Out	In	Out	In
48–56K	300000–337776	In	Out	Out	In
56–64K	340000–377776	Out	Out	Out	In
64–72K	400000–437776	In	In	In	Out
72–80K	440000–477776	Out	In	In	Out
80–88K	500000–537776	In	Out	In	Out
88–96K	540000–577776	Out	Out	In	Out
96–104K	600000–637776	In	In	Out	Out
104–112K	640000–677776	Out	In	Out	Out
112–120K	700000–737776	In	Out	Out	Out
120–128K	740000–777776	Out	Out	Out	Out

* W5 and W10 must be installed and W9 must be removed (for 8K stacks).

† The memory can be interleaved as 16K only, using two adjacent contiguously addressed 8K banks. When two 8K banks are interleaved, jumpers W7 and W8 must be in the configuration shown by the dotted lines. Bit A01 goes to the device selector gate controlled by jumper W6. One 8K bank must have W6 installed and the other must have W6 removed.
When not interleaved, jumpers W7 and W8 must be in the configuration shown by the solid lines. Bit A14 goes to the device selector gate controlled by jumper W6.



Non-Interleaved



Interleaved

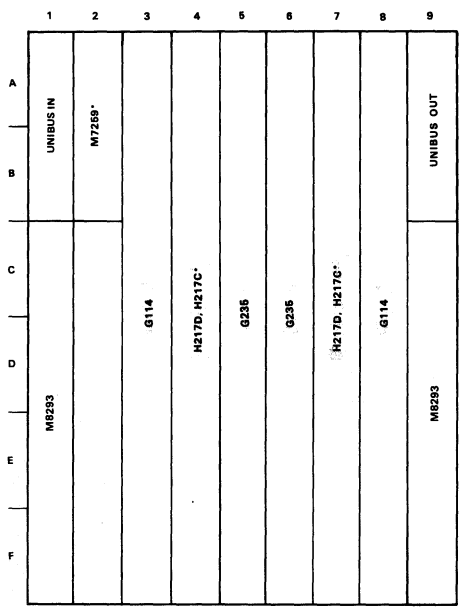
G110 CONTROL MODULE

NOTES:

1. Jumper W1 is for test purposes only. It must be installed for normal operation.
2. Jumper W11 should be removed for normal operation. When installed the memory responds to DATI only, regardless of state of control lines COO and CO1.
3. Jumpers W7 and W8 must remain in the factory installed positions.
4. When used as an 8k bank, jumpers W5 and W10 must be installed and jumper W9 must be removed.
5. When used as a 4k bank, jumper W10 must be removed and jumper W9 must be installed. Jumper W5 determines the location of the bank on the bus.

11-1149

MF11-U(P) MODULE UTILIZATION



* IF PARITY MEMORY.

M8293 DEVICE ADDRESS JUMPERS

Memory Bank (Words)	Machine Address (Words)$_8$	W7 A17	W6 A16	W5 A15	W4 A14	W3 A13
0–16K	000000–077776	IN	IN	IN	IN	IN
4–20K	020000–117776	IN	IN	IN	IN	OUT
8–24K	040000–137776	IN	IN	IN	OUT	IN
12–28K	060000–157776	IN	IN	IN	OUT	OUT
16–32K	100000–177776	IN	IN	OUT	IN	IN
20–36K	120000–217776	IN	IN	OUT	IN	OUT
24–40K	140000–237776	IN	IN	OUT	OUT	IN
28–44K	160000–257776	IN	IN	OUT	OUT	OUT
32–48K	200000–277776	IN	OUT	IN	IN	IN
36–52K	220000–317776	IN	OUT	IN	IN	OUT
40–56K	240000–337776	IN	OUT	IN	OUT	IN
44–60K	260000–357776	IN	OUT	IN	OUT	OUT
48–64K	300000–377776	IN	OUT	OUT	IN	IN
52–68K	320000–417776	IN	OUT	OUT	IN	OUT
56–72K	340000–437776	IN	OUT	OUT	OUT	IN
60–76K	360000–457776	IN	OUT	OUT	OUT	OUT
64–80K	400000–477776	OUT	IN	IN	IN	IN
68–84K	420000–517776	OUT	IN	IN	IN	OUT
72–88K	440000–537776	OUT	IN	IN	OUT	IN
76–92K	460000–557776	OUT	IN	IN	OUT	OUT
80–96K	500000–577776	OUT	IN	OUT	IN	IN
84–100K	520000–617776	OUT	IN	OUT	IN	OUT
88–104K	540000–637776	OUT	IN	OUT	OUT	IN
92–108K	560000–657776	OUT	IN	OUT	OUT	OUT
96–112K	600000–677776	OUT	OUT	IN	IN	IN
100–116K	620000–717776	OUT	OUT	IN	IN	OUT
104–120K	640000–737776	OUT	OUT	IN	OUT	IN
108–124K	660000–757776	OUT	OUT	IN	OUT	OUT
112–124K	700000–757776	OUT	OUT	OUT	IN	IN
116–124K	720000–757776	OUT	OUT	OUT	IN	OUT
120–124K	740000–757776	OUT	OUT	OUT	OUT	IN

NOTE: The memory may be interleaved in 32K increments, using two contiguously addressed 16K banks.

In the 16K interleaved memory configuration the following changes must be made:

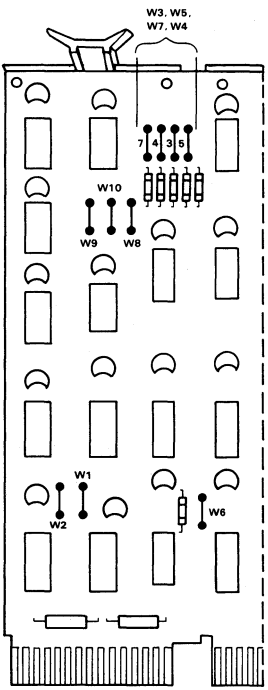
W1 is cut.
W2 is in.
W8 is in.
W9 is in. } For one 16K of the interleaved pair
W10 is cut. }
W9 is cut. } For the other 16K of the interleaved pair
W10 is in. }

Both interleaved memories should be cut for the same starting address.

Non-Interleaved

W1 is in.
W2, W8, W9, and W10 are cut.

M8293 16K UNIBUS TIMING MODULE



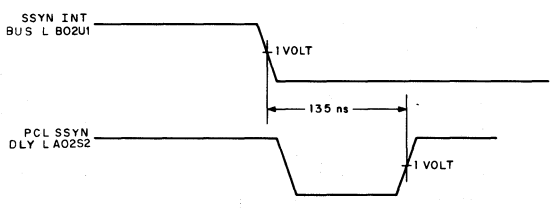
NOTE:

W1, W2, W8, W9, AND W10 ARE SELECTED FOR INTERLEAVED OR NON-INTERLEAVED OPERATION. W3, W4, W5, W6, AND W7 ARE SELECTED FOR STARTING ADDRESS

PCL SSYN DLY L ADJUSTMENT PROCEDURE FOR M7259 PARITY CONTROLLER

This adjustment sets a 105-ns delay from the leading edge of SSYN INT BUS L to allow sufficient settling time for the parity checking logic. Too long a delay will result in increased cycle time and access time. The waveshapes should be as shown below. Adjust R16 to obtain the required delay.

SSYN DLY L TIMING RELATIONSHIP



CSR ADDRESS JUMPER SELECTION FOR M7259 PARITY CONTROLLER MODULE,
Etch Rev D, CS Rev E

	CSR Jumpers	W4	W3	W2	W1
	Bus Address Line	A04	A03	A02	A01
Lower Memory Boundary	CSR Address				
0K	772100	X	X	X	X
4K	772102	X	X	X	O
8K	772102	X	X	X	O
12K	772104	X	X	O	X
16K	772104	X	X	O	X
20K	772106	X	X	O	O
24K	772106	X	X	O	O
28K	772110	X	O	X	O
32K	772110	X	O	X	X
36K	772112	X	O	X	O
40K	772112	X	O	X	O
44K	772114	X	O	O	X
48K	772114	X	O	O	X
52K	772116	X	O	O	O
56K	772116	X	O	O	O
60K	772120	O	X	X	X
64K	772120	O	X	X	X
68K	772122	O	X	X	O
72K	772122	O	X	X	O
76K	772124	O	X	O	X
80K	772124	O	X	O	X
84K	772126	O	X	O	O

(Continued)

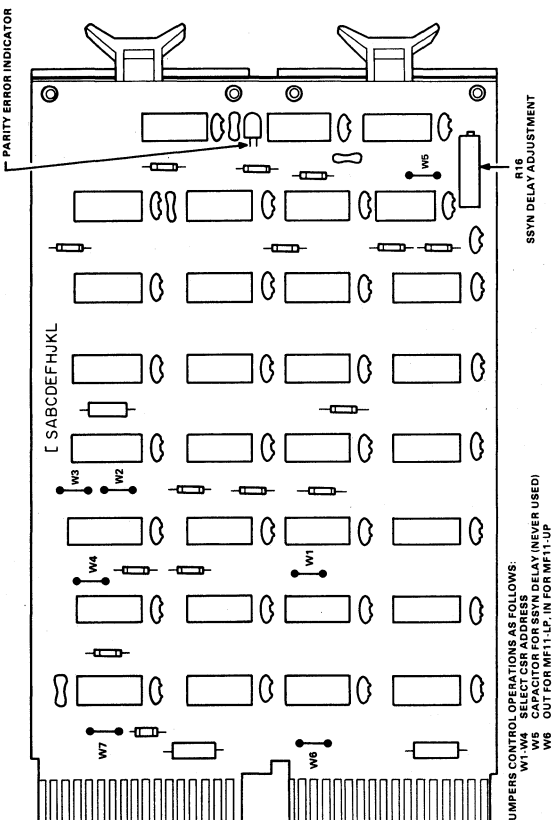
	CSR Jumpers	W4	W3	W2	W1
	Bus Address Line	A04	A03	A02	A01
Lower Memory Boundary	CSR Address				
88K	772126	O	X	O	O
92K	772130	O	O	X	X
96K	772130	O	O	X	X
100K	772132	O	O	X	O
104K	772132	O	O	X	O
108K	772134	O	O	O	X
112K	772134	O	O	O	X
116K	772136	O	O	O	O
120K	772136	O	O	O	O

O = Jumper Removed

X = Jumper Installed

W6: Removed for MF11-LP, installed for MF11-UP

M7259 PARITY CONTROL MODULE
(Etch Rev. D)



STROBE ADJUSTMENT PROCEDURE FOR MEMORIES USING THE G110

When any module in the memory system is replaced, the strobe must be adjusted for that system.

To adjust the strobe, use DZQMBC or a higher revision of the 0–124K Memory Exerciser MAINDEC.

Start the diagnostic at ADRS 214, allowing you to enter test parameters. Cycle on the bank to be adjusted while running pattern 1. Check program procedures for further information.

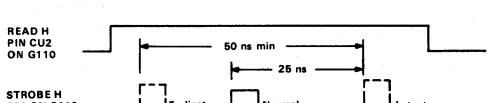
Attach and sync channel 1 to READ H pin CU2 of the G110 and channel 2 to STROBE H at test point 1 on the G110. (See the next page for the location of TP1.)

Adjust the strobe to the earliest (minimum) setting at which the memory will cycle error free and allow the test to run for three minutes.

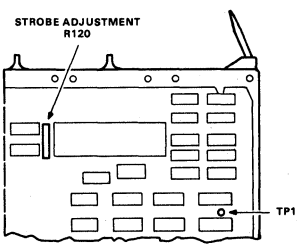
Adjust the strobe to the latest (maximum) setting at which the memory will cycle error free; this adjustment is most critical and there should not be more than 5 ns difference between the failing and passing points on this adjustment. Allow the test to run at this setting for three minutes or more.

This window should be 50 ns minimum. If it is not, replace modules within that bank of memory until it is.

Adjust STROBE H to be 25 ns (leading edge to leading edge) from the latest (maximum) setting.



G110 CONTROL MODULE



PDP-11/05 MAINTENANCE

The PDP-11/05 has the ability to run a program in its General Purpose registers. Therefore, disconnect all Unibus devices and all memory from the processor and if the console switches operate properly, attempt the program shown below.

General Purpose Register (GPR) Program

LOAD ADRS.....177700
DEPOSIT.....000240
000777
LOAD ADRS.....177700
START
The program is now being executed.
The run light should come on.
Press the HALT switch.
The ADDRESS/DATA display should contain either 177700 or 177701.

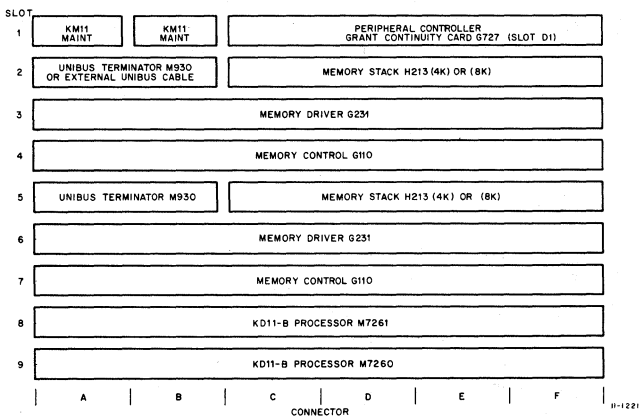
If a processor problem is indicated, replace the M7260 and M7261 modules, and attempt the failing procedure after each replacement.

Always replace *one* module at a time to ensure that you don't plug a module into the wrong slot. If you are not absolutely positive, check the module utilization diagrams in this DECAID.

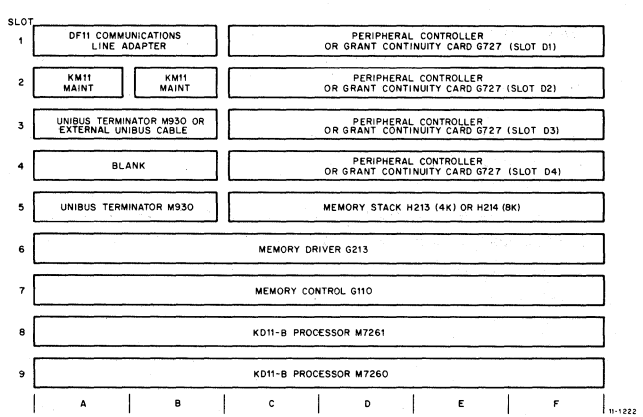
After replacing the M7260, it may be necessary to adjust the SCL clock as shown in this DECAID.

Remember, when you replace the M7261 module, check and if necessary, adjust the processor's clock rate as outlined in this DECAID.

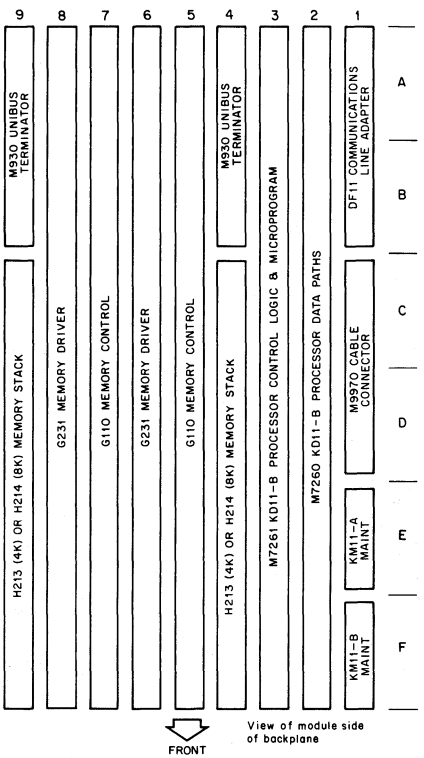
PDP-11/05-JA MODULE UTILIZATION (16K)



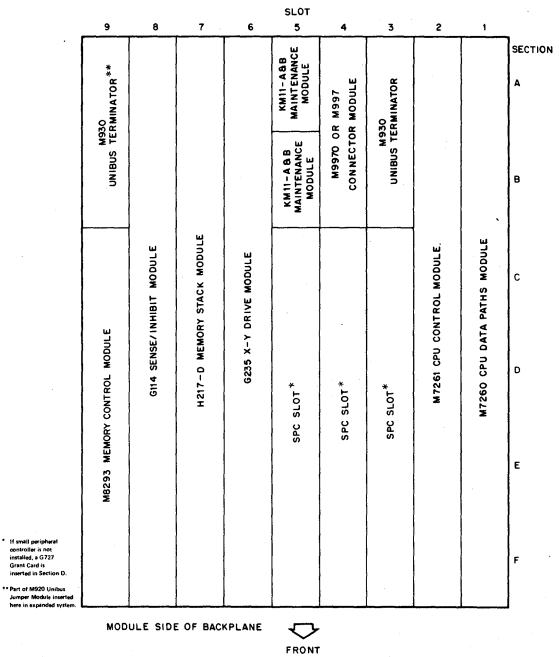
PDP-11/05-LA MODULE UTILIZATION (8K)



PDP-11/05-N MODULE UTILIZATION
(10-1/2-Inch Mounting Box)

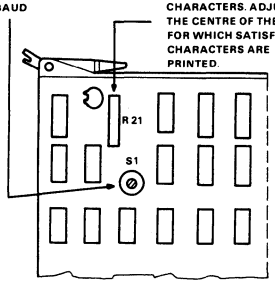


PDP-11/05/10-S MODULE UTILIZATION
(10-1/2-Inch Mounting Box)



M7260 DATA PATHS MODULE
(Etch Rev. C)

NOTES:
1. ARROW ON S1 MUST POINT TO:
   5 FOR 110 BAUD, 150 BAUD
   4 FOR 300 BAUD
2. RUN A PROGRAM TO PRINT A CONTINUOUS STREAM OF CHARACTERS. ADJUST R21 TO THE CENTRE OF THE RANGE FOR WHICH SATISFACTORY CHARACTERS ARE PRINTED.



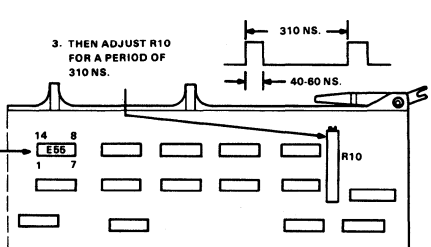
PROGRAM TO PRINT A STREAM OF CHARACTERS

500/005000	TOGGLE PROGRAM INTO CORE
502/105737	LOAD ADRS: 500
504/177564	START
506/100375	PROGRAM WILL LOOP
510/110037	CONTINUOUSLY UNTIL
512/177566	HALTED WITH HALT SWITCH
514/105200	
516/000771	

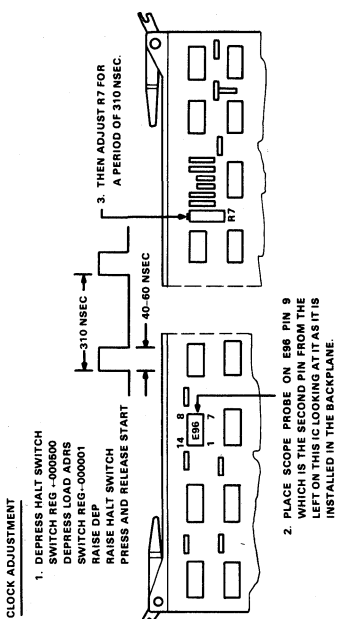
M7261 CONTROL LOGIC AND MICROPROGRAM MODULE
(Etch Rev. F)

CLOCK ADJUSTMENT

1. DEPRESS HALT SWITCH
   SWITCH REG ← 000500
   DEPRESS LOAD ADRS
   SWITCH REG ← 000001
   RAISE DEP
   RAISE HALT SWITCH
   PRESS & RELEASE START
2. PLACE SCOPE PROBE ON E55 PIN 8 WHICH IS THE FIRST PIN ON THE LEFT ON THIS IC LOOKING AT THE BOARD AS IT IS INSTALLED IN THE BACKPLANE
3. THEN ADJUST R10 FOR A PERIOD OF 310 NS.



M7261 CONTROL LOGIC AND MICROPROGRAM MODULE
(Etch Rev. E)



PDP-11/40 MAINTENANCE

The PDP-11/40 processor is comprised of the following modules:

M7231	Slot 4
M7232	Slot 3
M7233	Slot 5
M7234	Slot 7
M7235	Slot 6

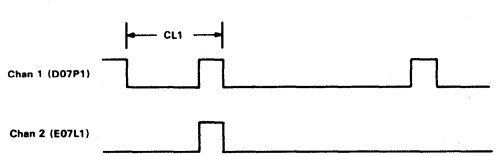
Always replace *one* module at a time to ensure that you don't plug a module into the wrong slot. If you are not absolutely positive where a module should go, check this DECAID for the module location.

Be very careful that the jumpers on the boards are cut and inserted correctly for the particular system you are working on. See this DECAID for a list of jumpers, their locations, and configurations.

When replacing the M7234 module, check and if necessary, adjust the processor's clock rate according to the following procedure.

Clock adjustment requires a dual-trace oscilloscope with channel 1 (triggering) on D07P1 and channel 2 on E07L1. The computer should be in the CONSOLE mode waiting for a switch activation. This may be forced by a START in the HALT mode. Make sure that both the RUN and CONSOLE lights are on. The S1 switch (see the M7234 module diagram in this DECAID for its location) is adjusted (in 10-ns increments) until the CL1 interval shown below is:

$\geqslant$140 ns $<$ 150 ns.



PDP-11/40 PROCESSOR MODULE'S JUMPERS

Option/ Module	KE11-E	KE11-F	KJ11	KT11-D	KW11-L	Parity Memory
M7231			Move: W2* (L→U)	Move: W10 (U→L) Cut: W1, W2, W3, W4, W5, W6, W7, W8, W9		
M7232						
M7233	Cut: W1†					
M7234			Move: W1 (U→L)	Move: W2 (L→U) Insert: C113, 680 pF C114, 560 pF		Cut: W5
M7235‡			Move: W1 (U→L)			Cut: W8
M7238		Cut: W1, W2, W3				
Backplane					Remove: Wire between pins F03R2 and F03V2	

Note: U = upper position and L = lower position between three split pins when looking at the module with the handles at the top. That is:

Upper position

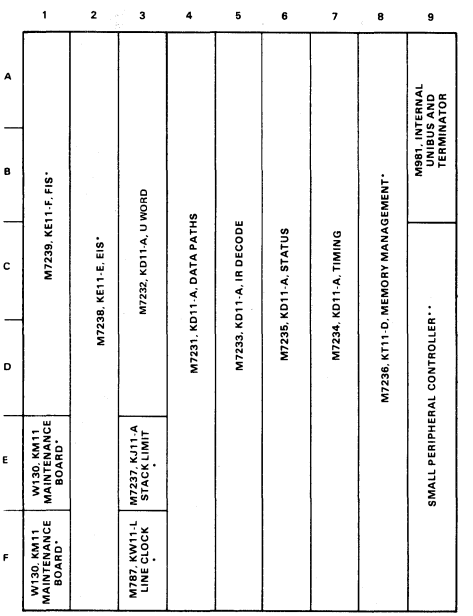
Lower Position

* If the KT11-D is installed along with the KJ11, cut the jumper out completely.

† Also install the three short cables between the M7232 and the M7238 modules.

‡ Connections for W7 through W2 are shown on the module for basic power-up vector address of 24_8. On the moudle's etch, the W numbers are located under these original jumper positions.

PDP-11/40 (KD11-A) MODULE UTILIZATION



NOTES:

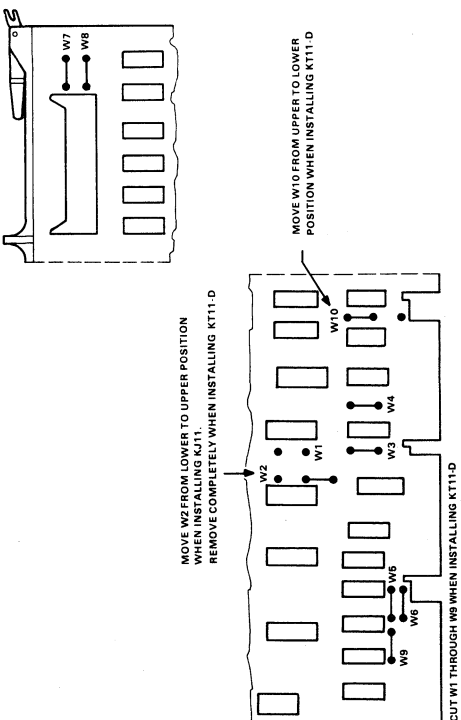
* PREWIRED MODULE SLOTS FOR NOTED OPTIONS.

** IF NO OPTION IS PRESENT IN THE SMALL PERIPHERAL CONTROLLER SLOT, A G727 GRANT CONTINUITY MODULE MUST BE INSERTED INTO ROW D.

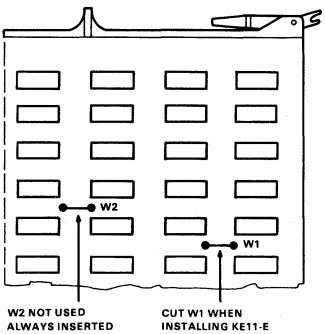
NOTE

As you are powering the machine on and off, one of the regulators may crowbar. You should suspect this if all the symptoms change for no apparent reason. If this should happen, determine which regulator has crowbarred, then turn its adjustment potentiometer a half revolution counterclockwise, and power the machine down and up. Then, with a scope, readjust the regulator so that it is producing the correct output. Remember that the machine must be powered down and up to turn the crowbar circuit off. Just turning the potentiometer down is not enough.

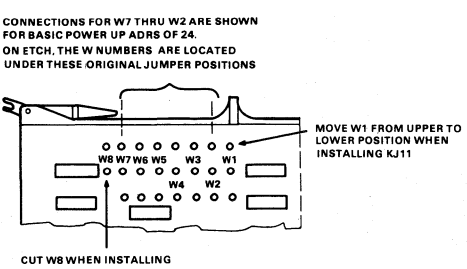
M7231 DATA PATHS MODULE
(Etch Rev. D)



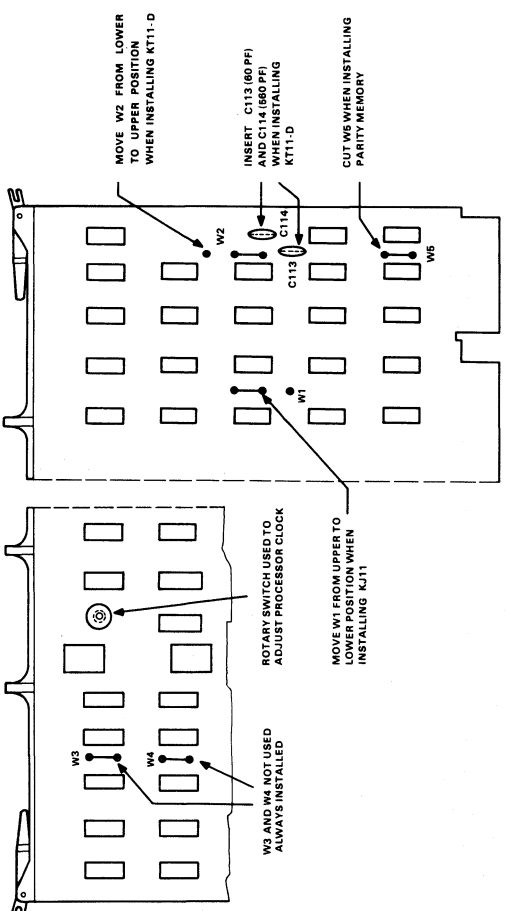
M7233 IR DECODE MODULE
(Etch Rev. D)



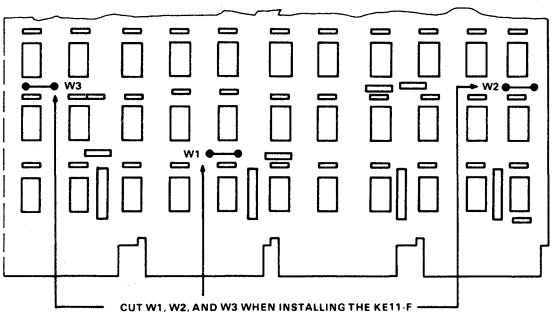
M7235 STATUS MODULE
(Etch Rev. D)



M7234 TIMING MODULE
(Etch Rev. D)



M7238 EIS MODULE
(Etch Rev. D)



PDP-11/45 MAINTENANCE

The PDP-11/45 processor is comprised of the following modules:

M8100	Slot 6
M8101	Slot 7
M8102	Slot 8
M8103	Slot 9
M8104	Slot 10
M8105	Slot 11
M8106	Slot 12
M8116	Slot 14 (if no Memory Management)
M8109	Slot 15

Always replace *one* module at a time to ensure that you don't plug a module into the wrong slot. If you are not absolutely positive where a module should go, check this DECAID for the module location.

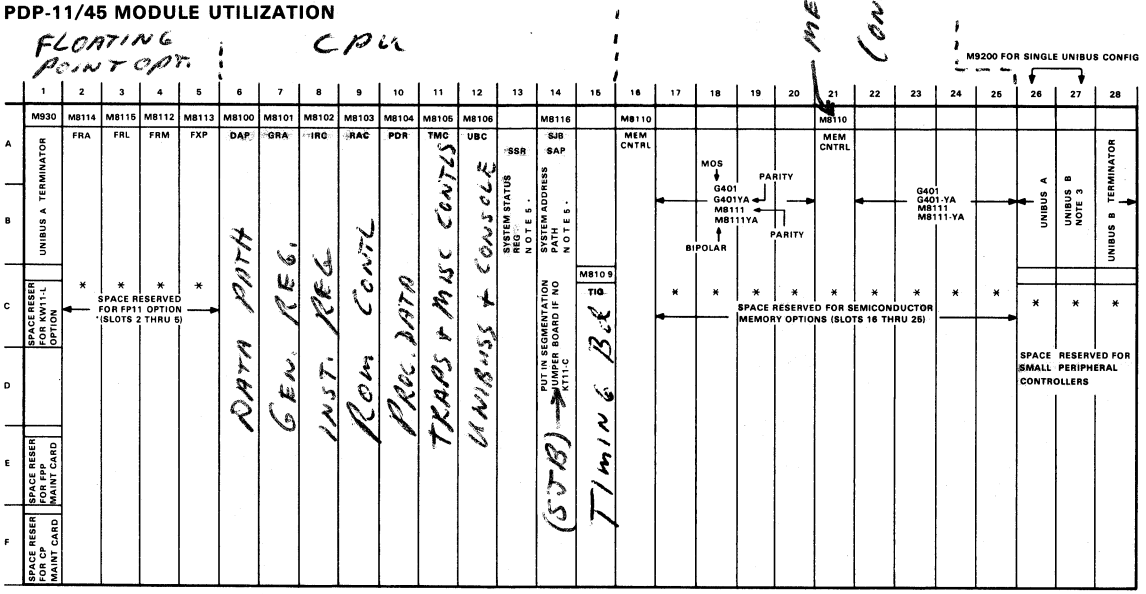
The PDP-11/45 has two 860 Power Controllers (one switched and one unswitched) or an 861 Power Controller with switched and unswitched outputs. Therefore, before you replace any modules, be sure to turn the power off at the power controller(s)' circuit breaker(s) not just at the front panel key. You might accidentally be changing a module that still has power applied to it.

When replacing the M8100, copy W1 through W6 from the old module onto the new module. See this DECAID for their location.

NOTE

As you are powering the machine on and off, one of the reulators may crowbar. You should suspect this if all the symptoms change for no apparent reason. If this should happen, determine which regulator has crowbarred, then rotate its adjustment potentiometer a half turn counter-clockwise and power the machine down and up. Then with a scope, readjust the regulator so that it is producing the correct output. Remember, the machine must be powered down to turn the crowbar off. Just turning the potentiometer down is not enough.

PDP-11/45 MODULE UTILIZATION



NOTES:

1. Power to MOS and BIPOLAR memory remains on with the console on/off switch in the off position. This is indicated by the LED on the MOS Control Board.

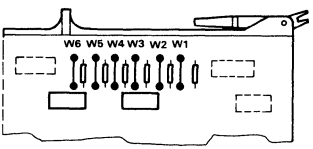
2. Caution must be observed when installing the boards into the backplane because of non-standard voltages present in slots 1, 2 and 15 thru 28.

3. If only one Unibus is used:
   The Unibus plugs into slot 28, plug an internal bus connector jumper (M9200) into slots 26 and 27, and plug a bus terminator (M930) into slot 1.
   If two Unibuses are used:
   Unibus A plugs into slot 26, terminator for Unibus A plugs into slot 1, Unibus B plugs into slot 27, and terminator for Unibus B plugs into slot 28.

4. Modules in slots 17-20 must be same type, modules in slots 22-25 must be same type.

5. If KT11 option is present, M8108 goes in slot 13 & M8107 goes in slot 14. If no KT11, M8116 goes in slot 14 and slot 13 is empty.

M8100 DAP MODULE
(Etch Rev. C)



W1 THRU W6 DETERMINE THE POWER UP VECTOR ADDRESS (USUALLY 24).

COPY FROM ORIGINAL MODULE.

CPU MODULES THAT DRIVE AND RECEIVE UNIBUS SIGNALS

CPU	Module	Unibus Signal
PDP-11/05	M7260	D<15:00>
	M7261	All the rest
PDP-11/40	M7231	A<17:00>, D<15:00>
	M7235	AC LO, DC LO, INIT, D<07:00>
	M7234	All the rest
PDP-11/45	M8104	D<15:00>
	M8116	A<17:00>
	M8105	BR<7:4>
	M8106	All the rest

BACKPLANE DC VOLTAGE CHECKS

With a calibrated scope, check the voltage levels and ripple on the backplane at the points indicated in the following tables. Notice that the tables indicate which regulator is providing the power being measured so that you can easily locate the correct one to adjust. (See DECAID PWRB-2 for the regulators' physical locations.)

Use a good scope probe with as short a ground lead as possible. Use "flag" type probe tips on both the scope probe and the ground lead and ground the probe on the backplane (not on the cabinet) as close as possible to the power point being measured.

CAUTION

Be extra careful that you put the ground lead on the correct backplane pin. Otherwise you may short something to ground which could cause considerable damage to the machine and your pride.

Only the voltage levels can be adjusted – not the ripple. If the magnitude of the ripple is greater than that specified, the offending regulator must be replaced.

PDP-11/40 CPU DC VOLTAGE CHECKS

Pin	Voltage (±5%)	Maximum Ripple (P-P Volts)	Regulator/ Slot
D09A2 (A01A2)	+5.0	0.20	H744/A
C09U1	+15.0	0.45	H742*
D09B2 (C09B2)	-15.0	0.45	H745/E

*No adjustment.

NOTE

If there is an MF11-U memory installed in the processor box, then all -15 V power must come from the H745 in slot D, since slot E contains the H754. Some configurations may have H754s in both slots D and E and then, of course, there cannot be anything installed in the box that requires -15 V, e.g., many small peripheral interfaces, MF11-L memories, etc.

PDP-11/45 CPU DC VOLTAGE CHECKS

Pin	Voltage	Maximum Ripple (P-P Volts)	Regulator/ Slot
A02A2	+5.0	0.20	H744/A (FPP)
F09V1	+5.0	0.20	H744/B (CPU)
F15V1	+5.0	0.20	H744/C (CPU)
F26A2	+5.0	0.20	H744/D (INT OPT)
E02B2	-15.0	0.45	H745/E (INT) (INT OPT and CPU)

(Continued)

Pin	Voltage	Maximum Ripple (P-P Volts)	Regulator/ Slot
A19A2	+5.0	0.20	H744/H (Bipolar)
A17V2	+23.2	0.70	H746/H (MOS)
A17U2	+19.7*	0.60	H746/H (MOS)
F17C1	-5.0	0.15	H746/H (MOS)
A16A2	+5.0	0.20	H744/J (MOS)
A21A2	+5.0	0.20	H744/K (Bipolar)
A24A2	+5.0	0.20	H744/L (Bipolar)
E15A1	+15.0† (13.5–16.5)	0.45	Top H742 (Switched)
E01B1	+8.0† (6.8–9.2)	0.24	Top H742 (Switched)
E16B2 E21B2	-15.0† (13.5–16.5)	0.45	Bottom H742 (Unswitched)

* 3 to 4 V less than +23.2.
† Not adjustable.

All voltages are to be adjusted to ±5% except +23.2 V, which is +3%, -5%.

REGULATOR SPECIFICATIONS

Regulator	Voltage and Tolerance	Output Current (Maximum)	P-P Ripple (Maximum)
H744	+5 Vdc ± 5%	25 A	200 mV
H745	-15 Vdc ± 5%	10 A	450 mV
H746	+23.2 Vdc +3, -5%	1.6 A	700 mV
	+19.7 Vdc	3.3 A (1)	700 mV
	-5 Vdc	1.6 A	150 mV
H754	+20 Vdc ± 5%	8 A	5% (3)
	-5 Vdc ± 5%	1 A–8 A (4)	5% (3)
H742	+15 Vdc ± 10%	3 A (2)	—
	+8 Vdc ± 15%	1 A (2)	—
	20–30 Vac (5 outputs)	300 W each output, 1 Kw max. total output.	—

Notes:

1. Refer to drawing D-CS-H746-0-1. Since the 19.7 V output is obtained by regulating down from the +23.2 V level, any combination of loads on the two outputs is acceptable as long as the sum does not exceed 5 A.

Notes (Cont):

Negative 5 V level is obtained by inserting a 5.1 V zener diode in series with the +23.2 and +19.7 loads, and using the zener cathode as GND. Therefore, maximum −5 V load current is equal to the greater of 1.6 A or the sum of the two positive load currents (+23 and +19).

2. Total not to exceed 3 A continuously.

3. At backplane. Typical ripple ≈±3%.

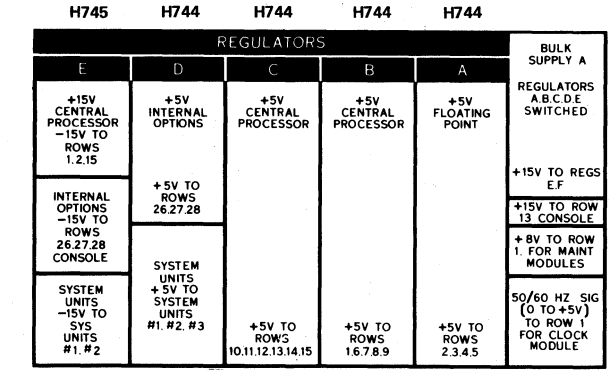
4. Maximum −5 V current is dependent upon +20 V current. It is equal to 1 A + I(+20) up to a total of 8 A. (I (+20) is the amount of +20 V current.)

PDP-11/40 REGULATOR/SLOT ASSIGNMENTS

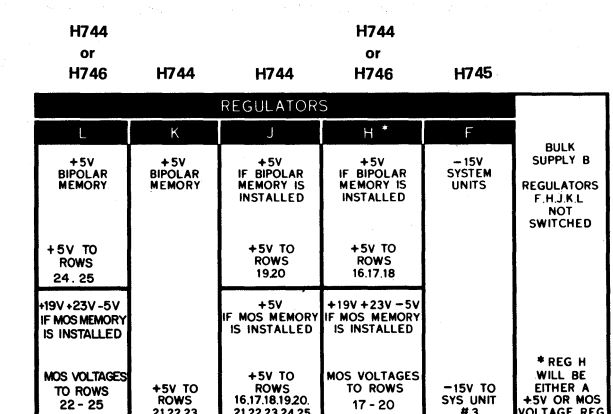
Regulators					H742 Bulk Power Supply
E	D	C	B	A	
H745 −15 V or H754 +20 V −5 V if MM11-U/UP	H745 −15 V or H754 +20 V −5 V if more MM11-U/UP	H744* +5 V	H744 +5 V	H744 +5 V	AC LO DC LO 20–30 Vac +15 V +8 V LTC

* Some earlier versions with small power requirements had no regulator in slot C.

PDP-11/45 REGULATOR SLOT ASSIGNMENTS
(Serial Numbers Beow 2000)



H742 Upper Power Supply



H742 Lower Power Supply

PDP-11/45 REGULATOR SLOT ASSIGNMENTS
(Serial Numbers 2000 and Higher)

H745 or H754	H744	H744	H744	H744	
REGULATORS					
E	D	C	B	A	H742 BULK SUPPLY
-15V TO SYSTEM UNITS 1 2 3	+5V INTERNAL OPTIONS -5V TO ROWS 26 27 28	+5V CENTRAL PROCESSOR	+5V CENTRAL PROCESSOR	+5V FLOATING POINT	-15V TO REGS E F ROW 13 & CONSOLE
+20V -5V ALTERNATE TO SYSTEM UNITS 1 2 3	-5V TO SYSTEM UNITS 1 2 3				ACLO DCLO +8V TO ROW 1 FOR MAINT MODULES
		-5V TO ROWS 10-15	-5V TO ROWS 1 6 7 8 9	+5V TO ROWS 2 3 4 5	50/60 HZ SIG (0 TO +5V) TO ROW 1 FOR CLOCK MODULE

H742 Upper Power Supply

H744 or H746	H744	H744	H744 or H746	H745	
REGULATORS					
L	K	J	H	F	H742 BULK SUPPLY
+5V BIPOLAR MEMORY +5V TO ROWS 24 25	+5V BIPOLAR MEMORY	+5V IF BIPOLAR MEMORY IS INSTALLED +5V TO ROWS 19 20	+5V IF BIPOLAR MEMORY IS INSTALLED +5V TO ROWS 16 17 18	+15V CENTRAL PROCESSOR -15V TO ROWS 1 2 15	-15V TO CENTRAL PROCESSOR
+19V +23V -5V IF MOS MEMORY IS INSTALLED		+5V IF MOS MEMORY IS INSTALLED	+19V +23V -5V IF MOS MEMORY IS INSTALLED	INTERNAL OPTIONS -15V TO ROWS 26 27 28 CONSOLE	
MOS VOLTAGES TO ROWS 22 - 25	+5V TO ROWS 21 22 23	+5V TO ROWS 16-25	MOS VOLTAGES TO ROWS 17 - 20		ACLO DCLO

H742 Lower Power Supply

PDP-11/45 VOLTAGE REGULATOR CONFIGURATION DATA CABINET SERIAL NUMBERS 2000 AND HIGHER

Type	Regulator Name	Quantity	Location	Comments
Basic System				
H744	+5 V	3	B	+5 V to CPU modules slots 6–9.
			C	+5 V to CPU and KT11-C modules, slots 10–15.
			D	+5 V to internal options, slots 26–28, system units 1, 2, and 3, and console.
H745	−15 V	1	F	−15 V to CPU and internal option modules. This supply is switched, even in the lower H742, because it is fed by +15 Vdc from the upper H742.
FP11-B Floating Point Processor				
H744	+5 V	1	A	+5 V to FP11 modules, slots 2–5.

PDP-11/45 VOLTAGE REGULATOR CONFIGURATION DATA CABINET SERIAL NUMBERS 2000 AND HIGHER (CONT)

Type	Regulator Name	Quantity	Location	Comments
MS11-C Bipolar Memory				
H744	+5 V	2	H, J	+5 V to control and matrix modules if no MOS memory is installed, or only 4K is used. H: slots 16–18; J: slots 19–20.
		2	K, L	If MOS memory is also installed, or if more than 4K of bipolar is used. K: slots 21–23, L: slots 24–25.
MS11-B MOS Memory				
H744	+5 V	1	J	+5 V to control and matrix modules, slots 16–25.
H746	MOS	2	H, L	+19.7 V, +23.2 V, and –5 V to MOS matrix modules; H slots 17–20; L slots 22–25.
MM11 Core Memories and Controls				
H745	–15 V	1	E	–15 V to system units 1–3.
H754	+20, –5 V	1	E	20 and –5 Vdc to MF11-U/UP. No –15 Vdc available for other system units.

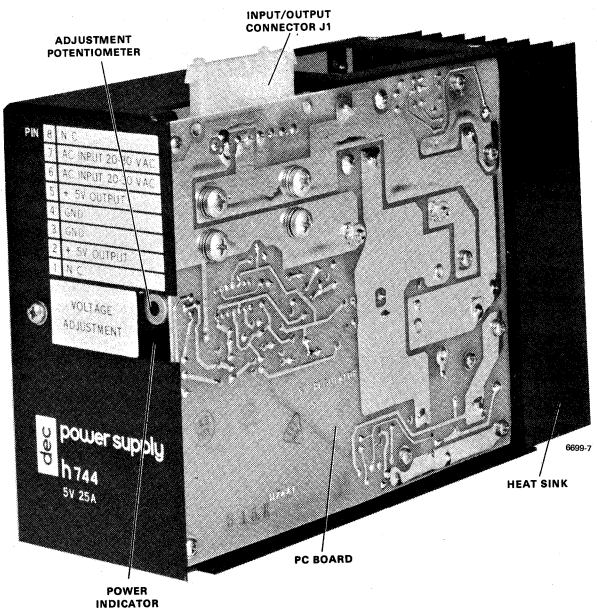
PDP-11/45 VOLTAGE REGULATOR CONFIGURATION DATA CABINET SERIAL NUMBERS LESS THAN 2000

Type	Regulator Name	Quantity	Location	Comments
Basic System				
H744	+5 V	3	B	+5 V to CPU modules, slots 6–9.
			C	+5 V to CPU and KT11-C modules, slots 10–15.
			D	+5 V to internal options, slots 26–28, system units 1, 2, and 3, and console.
H475	−15 V	1	E	−15 V to CPU and internal option modules and system units 1 and 2.
FP11-B Floating Point Processor				
H744	+5 V	1	A	+5 V to FP11 modules, slots 2–5.
MS11-C Bipolar Memory				
H744	+5 V	2	H, J	+5 V to control and matrix modules if no MOS memory is installed, or only 4K is used. H: slots 16–18; J: slots 19–20.

PDP-11/45 VOLTAGE REGLATOR CONFIGURATION DATA CABINET SERIAL NUMBERS LESS THAN 2000 (CONT)

Type	Regulator Name	Quantity	Location	Comments
		2	K, L	If MOS memory is also installed, or if more than 4K of bipolar is used. K: slots 21–23, L: slots 24–25.
MS11-B MOS Memory				
H744	+5 V	1	J	+5 V to control and matrix modules, slots 16–25.
H746	MOS	2	H, L	+19.7 V, +23.2 V, and –5 V to MOS matrix modules; H slots 17–20; L slots 22–25.
MM11 Core Memories and Controls				
H745	–15 V	1	F	–15 V to system unit 3. H745 provided in basic system supplies system units 1 and 2. This supply is switched even in the lower H742, because it is fed by +15 Vdc from the upper H742.

H744, +5 VDC REGULATOR



CROWBAR PROBLEMS

As you are powering the machine on and off (or for various other mysterious reasons), it can happen that one or more of the regulators may crowbar. That is, the regulator short circuits its output to protect the load. The output of a crowbarred regulator would be seen as approximately 0 V.

To check for this, first power the machine down. (This is very important; otherwise the crowbar circuit will not reset.) Then rotate the adjustment potentiometer of the offending regulator(s) counterclockwise a half revolution. Turn the power back on and observing the voltage level with a scope on the backplane pin, readjust the potentiometer so that the regulator is providing the correct output.

If you can't adjust the regulator's output to the correct level, then something else is causing the fault. Continue on the PWRB flows.

If you find that the regulator crowbars again after this procedure, then you have something connected to the regulator's output that is causing it to go too high. This is often due to a poor connection in one of the connectors in the power harness. Work the connectors firmly into their sockets and manipulate the wires going into the connectors.

Also look for possibilities such as a loose piece of wire shorting out a couple of backplane pins or else a backplane pin that is bent and is touching a neighboring pin.

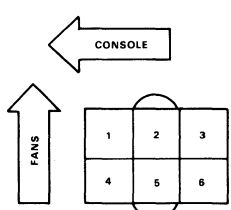
DISTRIBUTION PANEL CONNECTORS

The following diagrams show the locations of the pins carrying the power and signals into and out of the various distribution panels used on all models of the PDP-11/40 and PDP-11/45 processors.

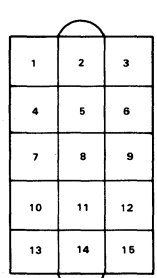
Check for these voltages by wedging the scope probe down into the connector's pin socket so that the probe makes connection with the pin inside the socket.

Note that the pin layout for the distribution panel supplying power to the system units on PDP-11/45s with serial numbers 2000 and higher is the same as the one for distribution panels used on PDP-11/40s with serial numbers 6000 and higher.

PDP-11/40 DISTRIBUTION PANEL CONNECTORS FOR SERIAL NUMBERS 6000 AND HIGHER



1. GND (BLK)
2. LINE CLK (BRN)
3. DC LO (VIO)
4. AC LO (YEL)
5. SPARE
6. SPARE

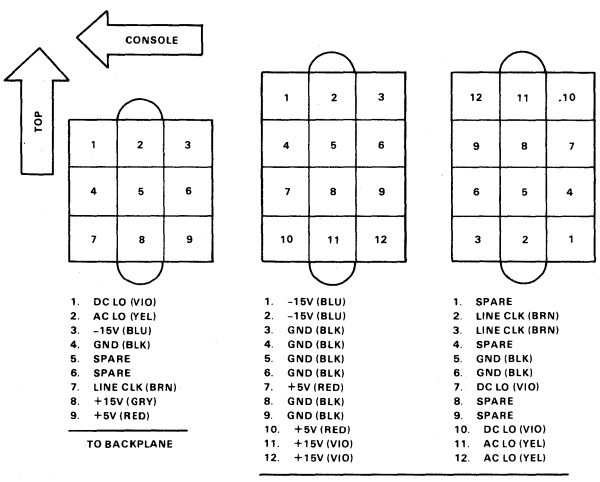


1. +5V (RED)
2. +15V (GRY)
3. +20V (ORN)
4. +5V (RED)
5. GND (BLK)
6. SPARE
7. GND (BLK)
8. GND (BLK)
9. GND (BLK)
10. SPARE
11. GND (BLK)
12. SPARE
13. -15V (BLU)
14. -5V (BRN)
15. SPARE

(Continued)

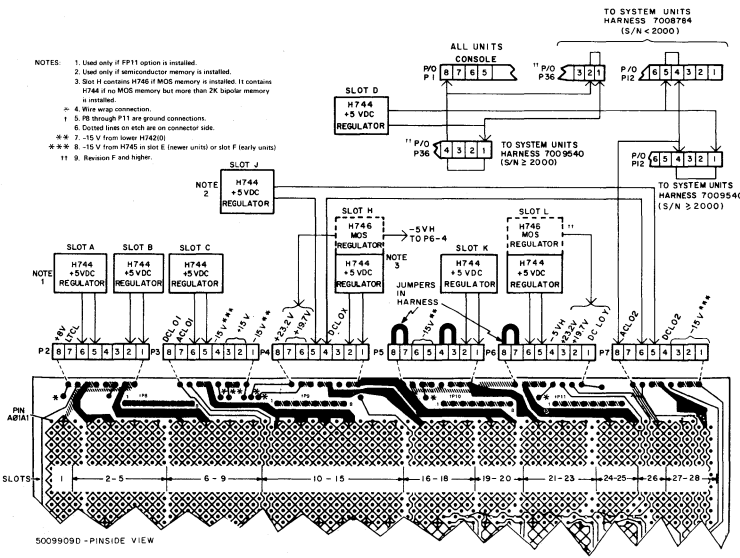
In the mainframe box's distribution panel there are four groups containing five pairs as shown above. Within a group, all pairs are bussed together pin-for-pin by the distribution panel. Each connector may or may not have all the above-listed wires connected to it.

PDP-11/40 DISTRIBUTION PANEL CONNECTORS FOR SERIAL NUMBERS LESS THAN 6000

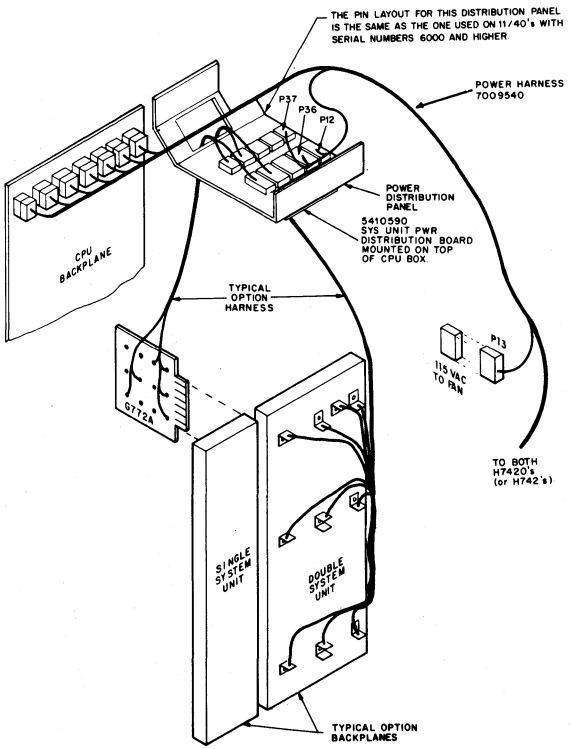


In the mainframe box's distribution panel, there are three groups each containing five connectors, that is, the two 12-pin connectors shown above and three of the 9-pin connectors shown above. Within a group, all three 9-pin connectors are bussed together pin-for-pin by the distribution panel. Each connector may or may not have all the above-listed wires connected to it.

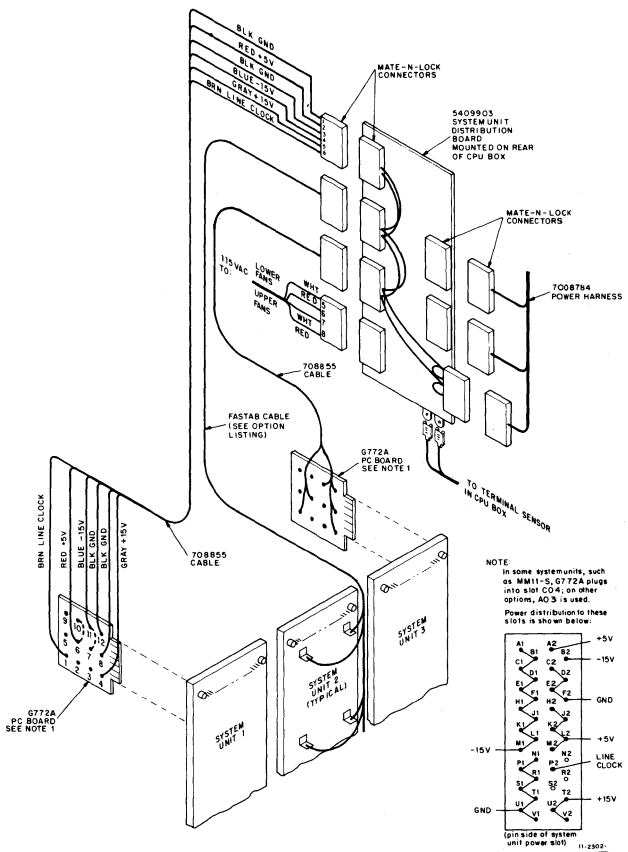
PDP-11/45 BACKPLANE CONNECTORS AND PINS



INSTALLATION OF SYSTEM UNITS, LATER SYSTEMS, PDP-11/45 CABINET SERIAL NUMBERS 2000 AND HIGHER



INSTALLATION OF SYSTEM UNITS, EARLY SYSTEMS, PDP-11/45 CABINET SERIAL NUMBERS LESS THAN 2000



POWER HARNESSES AND CABLES

Before you replace any of the cables or harnesses, ensure that the connectors are making a solid electrical connection. Firmly work the connectors into their sockets and manipulate the wires at the connectors while looking for any changes in the problem symptoms. If this procedure causes a change, then it may only be necessary to reset the connectors in their sockets or the pins in their connectors.

If you find that it is necessary to replace any cables, refer to the following pages of this DECAID to make sure that you obtain the correct replacement.

Present and future power handling capabilities of the 11/40-11/45 CP expander boxes and H960D, E cabinets have been increased with the creation of two new main power harnesses.

Along with this comes a whole new set of option cables necessary to connect our existing options to this new power configuration.

New and old machines may be easily identified by visually inspecting their serial number affixed to the expander box or by noting the new main power harness that is installed within the expander box.

Serial numbers > 6000 indicate a new PDP-11/40 power configuration (< = old type).

Serial numbers > 6000 indicate a new H960D, E power configuration (< = old type).

Serial numbers > 2000 indicate a new PDP-11/45 power configuration (< = old type).

The following tables list the options and CPU power harnesses affected by this change. Also included are the part numbers for other power cables not affected along with remote sense and intermodule cables used in the PDP-11 world.

POWER DISTRIBUTION HARNESS
(Power Supply to Distribution Points)

Description	Cable
PDP-11/15, PDP-11/20	70-6518
BA11-ES	70-5894
PDP-11/05 NC, PDP-11/35 10-1/2-inch box	70-9208
PDP-11/45, PDP-11/50 (Old)	70-8784
PDP-11/40 and H960D/E (Old)	70-8754
PDP-11/45 and PDP-11/50 (New)	70-9540
PDP-11/40 and H960D/E (New)	70-9566

* There will be some units between serial numbers 6000 and 6542 that will still have the old configuration.

DC DISTRIBUTION TO CPU BACKPLANE

Description	Cable
PDP-11/05S	70-9918
PDP-11/05 NC PDP-11/10 10-1/2-inch box	70-9360
PDP-11/35	70-9209
PDP-11/40 (Old)	70-9046
PDP-11/45	N/A
PDP-11/40 (New)	70-9564
PDP-11/35S	70-10113

NOTE

If a new PDP-11/35-PDP-11/40 backplane is ordered (part no. 70-10230), you must order 70-9994 cable for new-style PDP-11/40s. For old-style PDP-11/40s, use original cable cut to length.

REMOTE SENSE CABLES

Description	Cable
861 Remote Sense Cable (11/40 to 861)	70-9053
861/860 Remote Sense Cable (861/860 to 861/860)	70-8288
861/860 Remote Sense Cable (861/860 to 1st H720E/F)	70-8964
H720E/F to H720E/F Remote Sense Cable	70-8288
H720E/F (J2) Remote Sense Terminator Plug	70-7006-1
H720E/F (J1) Local Sense Jumper Plug	70-7006-2

INTER-MODULE CABLES

CPU Type	Description	Cable
PDP-11/05 (5-1/4 inch)	Console Cable	BC08R-3
PDP-11/05 (10-1/2 inch)	Console Cable	BC08R-4
PDP-11/35 PDP-11/35-11/40	Console to K1 and K5 (2) KE11-E (M7238 to M7232) (3)	BC08R-3 BC08R-1
PDP-11/40 PDP-11/45	Console to K1 and K5 (2) Console Cable (2)	BC08R-6 70-8864

OPTIONS

CPU Type Option	11/05, 11/10 10-1/2-In. Box	11/35 10-1/2-In. Box	11/35S, 11/05S BA11-KE/F 10-1/2-In. Box
AA11-DA	70-9205	70-9205	70-9562
AA11-DB	70-9205	70-9205	70-9562
DA11-F	70-9099	70-9099	70-10117
DB11-A	70-9205	70-9205	70-9562
DC11-A	70-9205	70-9205	70-9562
DD11-A	70-9205	70-9205	70-9562
DD11-B	70-9099	70-9099	70-10117
DH11-AA	N/A	N/A	70-10118
DH11-AB	N/A	N/A	70-10118
DH11-AC	N/A	N/A	70-10118
DJ11-AA	70-9099	70-9099	70-10117
DJ11-AB	70-9099	70-9099	70-10117
DJ11-AC	70-9099	70-9099	70-10117
DN11-AA	70-9205	70-9205	70-9562
DP11-DA	70-9205	70-9205	70-9562
DR11-B	70-9205	70-9205	70-9562
MF11-L	70-9206	70-9206	70-10114
MF11-LP	N/A	70-9206	70-10114
MF11-U/UP	N/A	N/A	70-10115
MM11-S	70-9205	70-9205	70-9562
RH11	70-9099	70-9099	70-9570
RH11-AB	70-9099	70-9099	70-10117
RK11-D	70-8992	70-8992	70-10116
VT11	70-9099	70-9099	70-10117
CD11-A/B/E	70-9099	70-9099	70-10117
DQ11	70-9099	70-9099	70-10117

OPTIONS

CPU Type Option	11/45 (Old)	11/40 H960D, E (Old)**	11/40, 11/45 H960D/E (New)
AA11-DA	70-8855-1J	70-8909-XX	70-9562
AA11-DB	70-8855-1J	70-8909-XX	70-9562
DA11-F	70-9162	70-9099	70-9563
DB11-A	70-8855-1J	70-8909-XX	70-9562
DC11-A	70-8855-1J	70-8909-XX	70-9562
DD11-A	70-8855	70-9177 70-8909-XX	70-9562
DD11-B	70-9162	70-9099	70-9563
DH11-AA	N/A	70-9466	70-9561
DH11-AB	N/A	70-9466	70-9561
DH11-AC	N/A	70-9466	70-9561
DJ11-AA	70-9162	70-9099	70-9563
DJ11-AB	70-9162	70-9099	70-9563
DJ11-AC	70-9162	70-9099	70-9563
DN11-AA	70-8855-1J	70-8909-XX	70-9562
DP11-DA	70-8855-1J	70-8909-XX	70-9562
DR11-B	70-8855-1J	70-8909-XX	70-9562
MF11-L*	70-9242	70-9103	70-9565
MF11-L†	N/A	70-9174	70-9560
MF11-LP*	70-9242	70-9103	70-9565
MF11-LP†	N/A	70-9174	70-9560
MF11-U/UP‡	N/A	N/A	70-9535
MM11-S	70-8855-2B	70-8909-XX	70-9562
RH11	70-9162	70-9571	70-9570
RH11-AB	70-9162	70-9099	70-9563
RK11-D	70-8855-1J	70-8992	70-9559
VT11	70-9162	70-9099	70-9563
CD11-A/B/E	70-9162	70-9099	70-9563
DQ11	70-9162	70-9099	70-9563

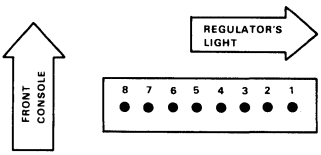
* PDP-11/40 only (1st MF11-L/LP).

† PDP-11/40 only (2nd MF11-L/LP).

‡ MF11-U/UP cannot be mounted in old style PDP-11/45 CPU box.

** 70-8909-XX cable has two variations – 11 inches and 17 inches. Use 70-9177 if due to new module guide layout; 70-8909-XX cables are too short.

PIN LOCATIONS FOR REGULATOR'S CONNECTORS



H744

1. Spare
2. +5 V output (red)
3. GND (black)
4. GND (black)
5. +5 V output (red)
6. 20–30 Vac input (red)
7. 20–30 Vac input (white)
8. Spare

H745

1. –15 V output (blue)
2. GND (black)
3. GND (black)
4. +15 V input (violet or gray)
5. +15 V input (violet or gray)
6. 20–30 Vac input (red)
7. Spare
8. 20–30 Vac input (white)

H754

1. Spare
2. GND (black)
3. –5 V output (brown)
4. Spare
5. +20 V output (orange)
6. Spare
7. 20–30 Vac input (red)
8. 20–30 Vac input (white)

H746

1. Spare
2. GND
3. –5 V output
4. +19.7 V output
5. +23.2 V output
6. Spare
7. 20–30 Vac input
8. 20–30 Vac input

PROCEDURE FOR REMOVAL OF REGULATORS

1. Turn the power off at the circuit breaker on the 860/861 Power Controller.

2. Disconnect the connector at the top of the regulator.

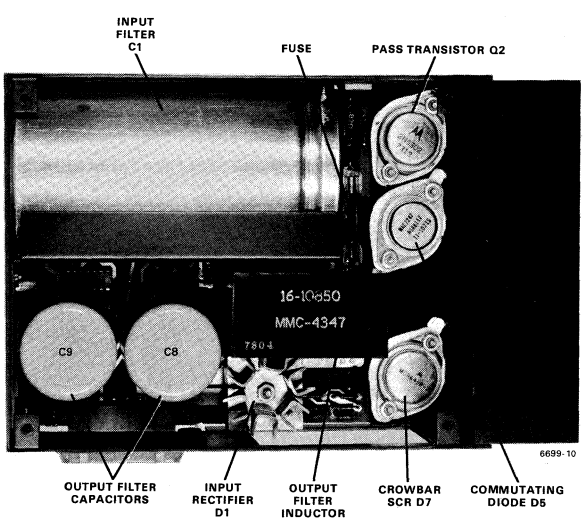
3. Remove the two Phillips screws on top of the regulator which hold the regulator in the H742 box.

4. Loosen the finger-tight (usually) screw on the bottom of the regulator.

5. Slide the regulator out horizontally away from the H742 box.

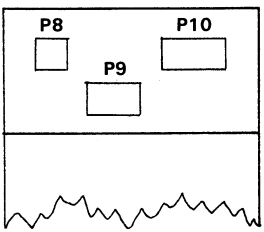
The following diagram shows the location of the fuse. Usually you can check it without taking off the clear plastic cover. It is an AGC 15-amp fuse.

+5 V REGULATOR, SIDE VIEW



H742 CONNECTORS FOR PDP-11/40

As seen from the back, the connectors on the H742 Power Supply are located as shown in the diagram below.



The following pages list the functions and locations of each of the pins on the above three connectors.

PDP-11/40 Pin Locations for H742's Connectors

P8

3	6	9
2	5	8
1	4	7

Pin(s)	Function (Vac)	Color	Dest.
1–2 (new)	20–30	Red, white	Slot B
1–2 (old)	20–30	Red, white	Slot A
3–4	20–30		
5–6	20–30		
7–8	20–30	Red, white	Slot D

PDP-11/40 Pin Locations for H742's Connectors (Cont)

P9

3	6	9	12
2	5	8	11
1	4	7	10

Pin(s)	Function	Color	Dest.
1	+8 V		
2	+15 V	Gray or violet	Dist. Panel
3	+15 V	Gray or violet	Slot D
4	GND	Black	Slot D
5	GND	Black	Slot E
6	GND	Black	Dist. Panel
7	GND	Black	Dist. Shield
8	AC LO	Yellow or red	Dist. Panel
9	DC LO		
10	AC LO		
11	LINE CLK	Brown or black	Dist. Panel
12	DC LO	Violet or clear	Dist. Panel

PDP-11/40 Pin Locations for H742's Connectors (Cont)

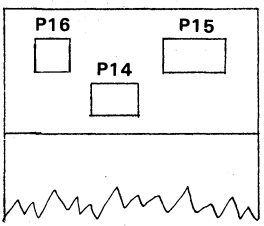
P10

3	6	9	12	15
2	5	8	11	14
1	4	7	10	13

Pin(s)	Function (Vac)	Color	Dest.
1–2 (new)	20–30	Red, white	Slot A
1–2 (old)	20–30	Red, white	Slot B
8–10	20–30	Red, white	Slot C
9–12	20–30	Red, white	Slot E
3–7	115	Red, white	H742 fan
5–6	115	Red, white	Proc. fans

UPPER H742 CONNECTORS FOR PDP-11/45

As seen from the back, the connectors on an upper H742 Power Supply are located as shown in the diagram below.



The following pages list the functions and locations of each of the pins on the above three connectors.

PDP-11/45 Pin Locations for Upper H742's Connectors

P16

3	6	9
2	5	8
1	4	7

Pin(s)	Function (Vac)	Color	Dest.
1–2	20–30		
3–4	20–30	Red, white	Slot B
5–6	20–30		
7–8	20–30	Red, white	Slot C

PDP-11/45 Pin Locations for Upper H742's Connectors (Cont)

P14

3	6	9	12
2	5	8	11
1	4	7	10

Pin(s)	Function	Color	Dest.
1	+8 V	White	Dist. Panel
2 (new)	+15 V	Gray	Slot F
2 (old)	+15 V	Gray	Slot E
3	+15 V	Gray	Dist. Panel
4	GND	Black	Slot E
5	GND	Black	Dist. Panel
6	GND	Black	Slot F
7	GND	Black	Dist. Panel
8	AC LO	Yellow	Dist. Panel
8	AC LO	Yellow	Lower H742
9 (new)	DC LO		
9 (old)			
10	AC LO	Yellow	Dist. Panel
10	AC LO	Yellow	Lower H742
11	LINE CLK	Brown	Expn. Dist.
12	DC LO	Violet	Dist. Panel

PDP-11/45 Pin Locations for Upper H742's Connectors (Cont)

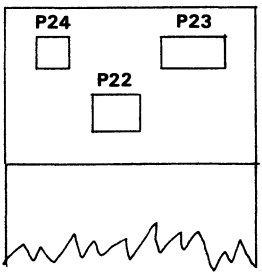
P15

3	6	9	12	15
2	5	8	11	14
1	4	7	10	13

Pin(s)	Function (Vac)	Color	Dest.
1–2	20–30	Red, white	Slot A
8–10	20–30	Red, white	Slot D
9–12	20–30	Red, white	Slot E
3–7	115	Red, white	H742 fan
5–6	115	Red, white	Time meter

LOWER H742 CONNECTORS FOR PDP-11/45

As seen from the back, the connectors on a lower H742 Power Supply are located as shown in the diagram below.



The following pages list the functions and locations of each of the pins on the above three connectors.

PDP-11/45 Pin Locations for Lower H742's Connectors

P24

3	6	9
2	5	8
1	4	7

Pin(s)	Function (Vac)	Color	Dest.
1–2	20–30	Red, white	Slot J
3–4	20–30		
5–6	20–30	Red, white	Slot H H746
7–8	20–30	Red, white	Slot H H744

PDP-11/45 Pin Locations for Lower H742's Connectors (Cont)

P22

3	6	9	12
2	5	8	11
1	4	7	10

Pin(s)	Function	Color	Dest.
3	GND	Black	Dist. Panel
4	−15 V	Blue	Dist. Panel
7	GND	Black	Dist. Panel
8	AC LO	Yellow	Upper H742
9	DC LO	Violet	Dist. Panel
10	AC LO	Yellow	Upper H742
12	DC LO	Violet	Dist. Panel

PDP-11/45 Pin Locations for Lower H742's Connectors (Cont)

P23

3	6	9	12	15
2	5	8	11	14
1	4	7	10	13

Pin(s)	Function (Vac)	Color	Dest.
1–2	20–30	Red, white	Slot L
8–10	20–30	Red, white	Slot K
9–12	20–30	Red, white	Slot F
5–6	115	Red, white	Proc. fans
3–7	115	Red, white	H742 fan

PROCEDURE TO CHECK THE FUSE AND TO REMOVE THE POWER CONTROL BOARD WITHIN THE H742 POWER SUPPLY

CAUTION

You are working with 115 Vac. Be very sure to disconnect the H742 from the power source and allow about 10 seconds for the capacitors to discharge before starting this procedure.

Lift off the H742's top and side cover (one piece) after removing the two screws located at the front and rear of the power supply box. Don't pull it away too far as the fan on the cover is conncted to a terminal board in the box.

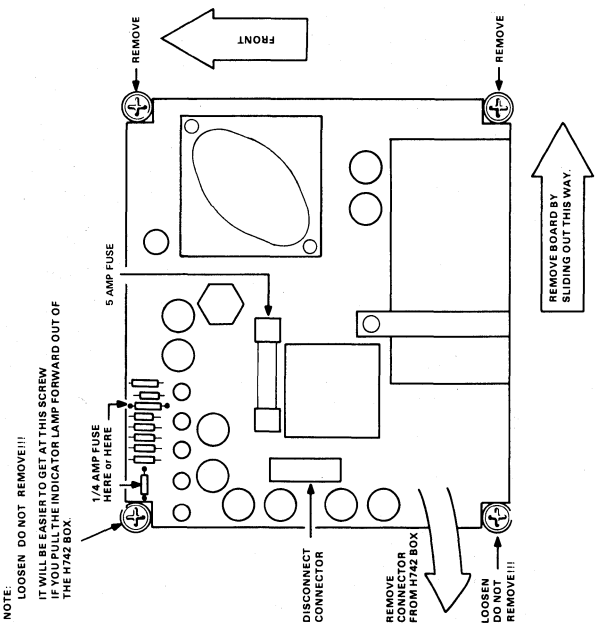
Check the fuses (5 amp and 1/4 amp) on the power control board. The following diagram shows their locations.

If it is necessary to replace the power control board:

- Loosen but **do not remove*** the two screws indicated in the diagram.
- Remove the screws indicated.
- Disconnect the connector from the board.
- Remove the other connector from the box.
- Slide out the power control board.

* Do not remove these screws because it is very likely that in trying to put them back in, you will drop them down into the H742 box.

H742'S POWER CONTROL BOARD



PDP-11/05/10 POWER CONNECTORS

See the next page for a diagram shownin the pin locations.

PDP-11/05/10 5-1/4-INCH BOX

Voltage	Tolerance	Allowable Ripple
+15 V	±5%	750 mV
+5 V	±5%	200 mV
-15 V	±5%	450 mV

PDP-11/05-N, 11/10-N 10-1/2-INCH BOX

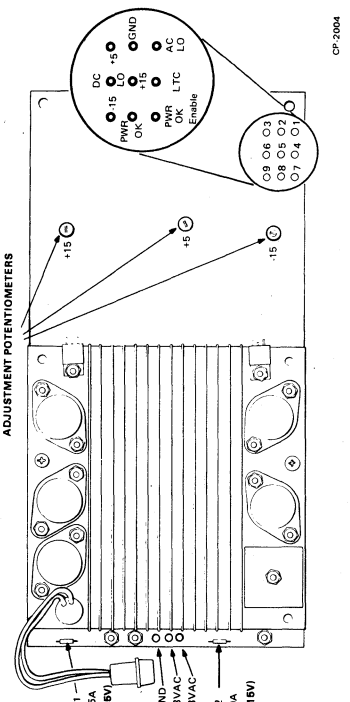
Voltage	Tolerance	Allowable Ripple	Regulator
+15 V	±5%	500 mV	5409728
+5 V	±5%	200 mV	5409728
-15 V	±5%	450 mV	5409728
+5 V	±5%	200 mV	H744

The two +5 V outputs must *not* be shorted together. The 5409728 regulator provides +5 V to connectors J1 and J2 on the power distribution board. The H744 provides +5 V to connectors J3, J4, and J5. The CPU backplane is normally connected to J1.

PDP-11/05-S, 11/10S

Voltage	Tolerance	Allowable Ripple	Wire Color	Pin Number
+5 V	±5%	200 mV	Red	1, 4
+15 V	±10%		Gray	2
+20 V	±5%	100 mV	Orange	3
-15 V	±5%	450 mV	Blue	13
-5 V	±5%	250 mV	Brown	14

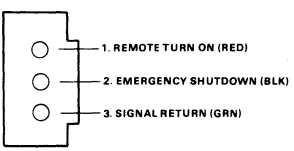
54-09728 POWER REGULATOR



REMOTE POWER CONTROL FACILITY

All PDP-11 computers have provisions to allow the console switch to control the operation of the cabinet mounted 860/861 Power Controllers and H720 Power Supplies.

These devices should be connected together with the remote power control bus which is a 3-wire system with the wires having the functions shown below:



POWER CONTROL OPERATION

Connections Between Control Lines	Switch Position		
	Local Switched Power Is	Off Switched Power Is	Remote Switched Power Is
None	On	Off	Off
1–3	On	Off	On
2–3	Off	Off	Off
1–3, 2–3	Off	Off	Off

See DECAID PWRB-5 for a list of the remote sense cables used to connect various power components.

SUGGESTIONS ON WHAT TO DO BEFORE ACTUAL HARDWARE TROUBLESHOOTING

Before you go to the customer's site:

1. Find out as much about the system configuration as you can.

   - Which CPU
   - How much memory, what type
   - What mass storage devices, how many of each
   - What software
   - What other peripherals, how many of each
   - What communications equipment, etc.

2. Read the last few Field Service Reports for this system to see if the problem is a recurring one or if it may be related to some work that was done recently.

When you get to the customer's site:

1. Question (gently) the user to find out as much about the failure as possible.

   - What was the system doing when it failed?
   - Was there any smoke, sparks, noises, etc.?
   - What software was running?
   - How many users were on the system?
   - Have there been any recent changes to the hardware or software?

2. Check the obvious and simple possibilities first.

   - Power plugs not inserted properly
   - Cables hanging loose
   - Physical damage